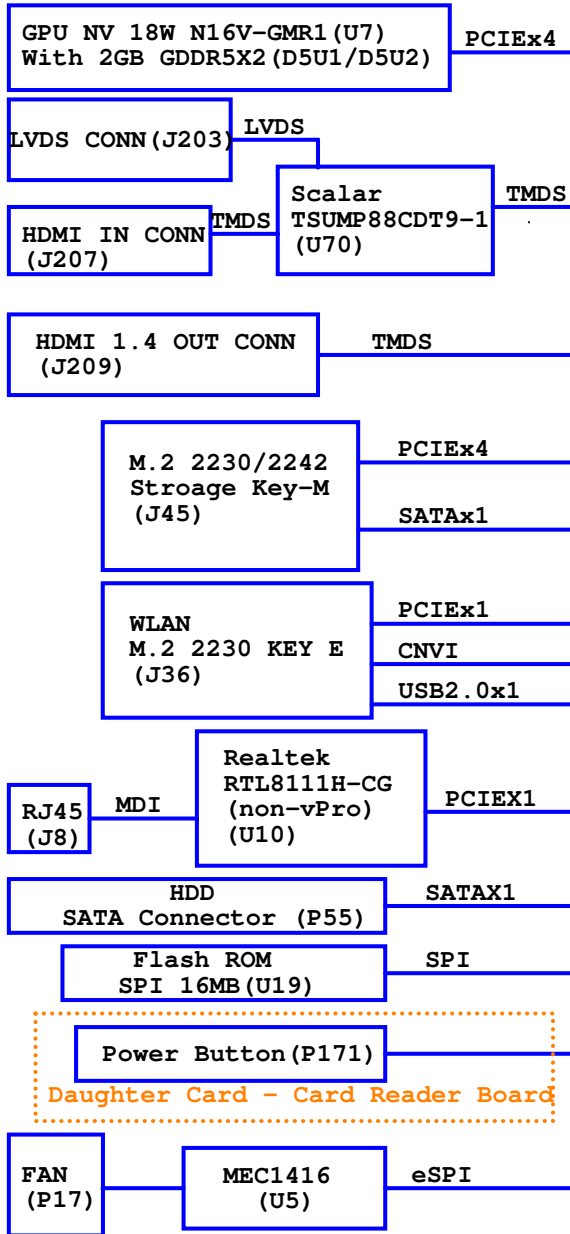
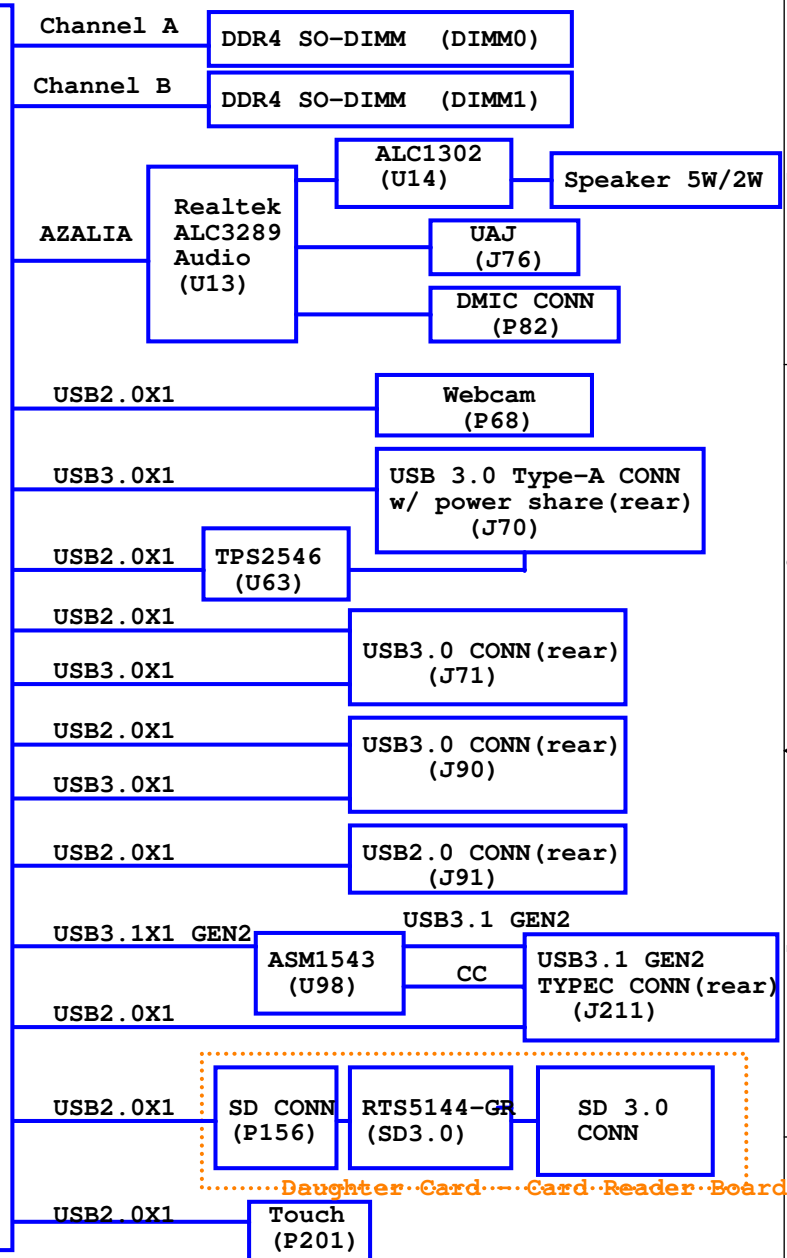


IPCML-CL CML-U

PAGE	TITLE
01	BLOCK DIAGRAM
02	POWER SEQUENCE
03	POWER FLOW CHART
04	CLOCK DISTRIBUTION
05	GPIO TABLE 1-2
06	GPIO TABLE 2-2
07	SMBUS MAP
08	WHL U DISPLY
09	WHL U DDR4
10	WHL U LPSS/ISH
11	WHL U PCIE/USB
12	WHL U CLOCK
13	WHL U AUDIO/SDIO
14	WHL U SPI/SMB/LPC
15	WHL U CSI/EMMC/CNV
16	WHL U SYS PWR CONTR
17	WHL U MISC/JTAG/CLK
18	WHL U VCCPRIM/VCCAPLL
19	WHL U VDDQ/VCCIO/VCCSA
20	WHL U VCORE/VCCGT
21	WHL U VCORE/VCCGT CAP
22	WHL U GND
23	WHL U RESERVED
24	DDR4 SO-DIMM CHA
25	DDR4 SO-DIMM CHR
26	RTC
27	SPI ROM(16MB)
28	XPE/ESPI DEBUG
29	MICROCHIP MEC1416 1-2
30	MICROCHIP MEC1416 2-2
31	PCH DEWROK
32	USB 3.0 CHARGING PORT
33	USB 3.0 PORT
34	USB 3.0 PORT
35	USB 2.0 PORT
36	USB 3.1 GEN2 MUX ASM1543
37	USB TYPE C CONNECTOR
38	TOUCH/WEBCAM
39	LAN RTL8111HSD-CG
40	LAN JACK
41	SSD M.2 KEY M
42	WLAN M.2 KEY E
43	AUDIO CODEC ALC3289
44	AMP ALC 1302
45	AUDIO CONNECTOR
46	HDD/FAN/Card/PWR BTN
47	Discharge/SCREW
48	HDMI OUT
49	SCALAR IC
50	SCALAR POWER
51	SCALAR HDMI IN
52	SCALAR MISC 1-2
53	SCALAR MISC 2-2
54	FHD LVDS CONNECTOR
55	XXXXXXXXXX
56	N16V-GMR1 PCIE INTERFACE
57	N16V-GMR1 FRAME BUFFER
58	N16V-GMR1 DAC A_XTAL
59	N16V-GMR1 TFP NC
60	N16V-GMR1 GPIO
61	N16V-GMR1 Power_GND
62	N16V-GMR1 STRAP
63	N16V-GMR1 FB[0_31]
64	N16V-GMR1 FB[32_63]
65	N16V-GMR1 SEQUENCE
66	XXXXXXXXXX
67	XXXXXXXXXX
68	TP PCB Label
69	DEBUG LED
70	UVP_OVP +19VSB
71	OPTIMIZER/PSID
72	+5VSB TP
73	+5VSB +3P3VA_3VA_5VA
74	CPU CONTROLLER
75	+VCORE DRIVER
76	+VCCGT DRIVER
77	+VCORE & +VCCGT CAP
78	+VCCSA DRIVER & CAP
79	XXXXXXXXXX
80	+0P9V CPUIO
81	+1P2V DUAL +0P6V_VTTDDR
82	+2P5VFP
83	+1P05VSB
84	+1P8VSB
85	19V_VCCST_VCCSTG_1P2V
86	3VSB_3V WLAN SSD LAN_FAN
87	5V_1P2V_SCL_5V HDD
88	+NVVDD CONTROLLER
89	+NVVDD DRIVER
90	+1P35V FBVDDQ
91	+1P05V GPU/+3P3V GPU
92	CONVERTER BOARD
93	XXXXXXXXXX
94	XXXXXXXXXX
95	XXXXXXXXXX
96	POWER BUTTON BOARD
97	CHANGE HISTORY



INTEL
CML-U
TDP 15W





POWER FLOW

Adapter

Current Limit
CY8C4125RT3602AHGQW + RT9610CGQW*1
IA--2ph --- 5x6, FlipChip Dual-N, 8m/1.8m
GT--1ph --- 5x6, P-PAK, 9m/6m/6m
SA--1ph --- 2x2, P-PAK, 25m

NB681AGD-Z

RT8231A
5x6, P-PAK, 9m/6m/6m5x6, P-PAK, 9m/6m
RT6575B
3x3, P-PAK, 14mRT8237EZQW
3x3, P-PAK, 27m/9.8mRT8812AGQW
5x6, P-PAK, 9m/6m

APW8714EQBI-TRG

RT8231B

APL3523AOB

RT6575B

APL3523AOB

APL3523AOB

RT5797A

APL5934D

NMOS SOT-23

RT6575B

APL3523AOB

APL3523AOB

APL3523AOB

NMOS SOT-23

APL3523AOB

APL3523AOB

APL5934D

APL3523AOB

SI7121DN-T1

+V CORE CML-U15

+VCCGT CML-U15

+VCCSA CML-U15

+VCCIO Imax=4.079A

+1P2V_DUAL Imax=11.42A

+0P6V_VTDDR Imax=0.7A

+1P2V_SCL Imax=0.206A

+5VAR Imax=0.014A

+5VSB Imax=8A

+5V_FAN Imax=0.5A

+5V_HDD Imax=1.5A

+5V Imax=2A

+1P8VSB Imax=0.712A

+1P05V_GPU Imax=0.8A

+1P8V Imax=0.071A

+3P3VAR Imax=0.01A

+3P3VA Imax=0.204A

+3P3V Imax=1.006A

+3P3VSB_LAN Imax=1.5A

+3P3V_WLAN Imax=2A

+3P3V_SSD Imax=3A

+3P3V_SCL Imax=0.165A

+3P3V_HDD Imax=1A

+3P3V_MAIN Imax=0.1A

+3P3V_AON Imax=0.1A

+3P3VSB Imax=0.258A

+2P5VPP Imax=1.58A

+1P05VSB Imax=10A

+1P05V_ST Imax=0.21A

+1P05V_STG Imax=0.02A

+NVVDD Imax=31A

+FBVDDQ Imax=4.24A

+19V Imax=2.26A

Switching

Linear

SPDT/Switch

PEGATRON Title :003 - POWER FLOW

PEGATRON CORPORATION		Engineer: Jayjay Peng	
Size	Project Name	Rev	Rev
Custom	IPCML-CL	A00	
Date: Thursday, July 25, 2019	Sheet	3	of 97



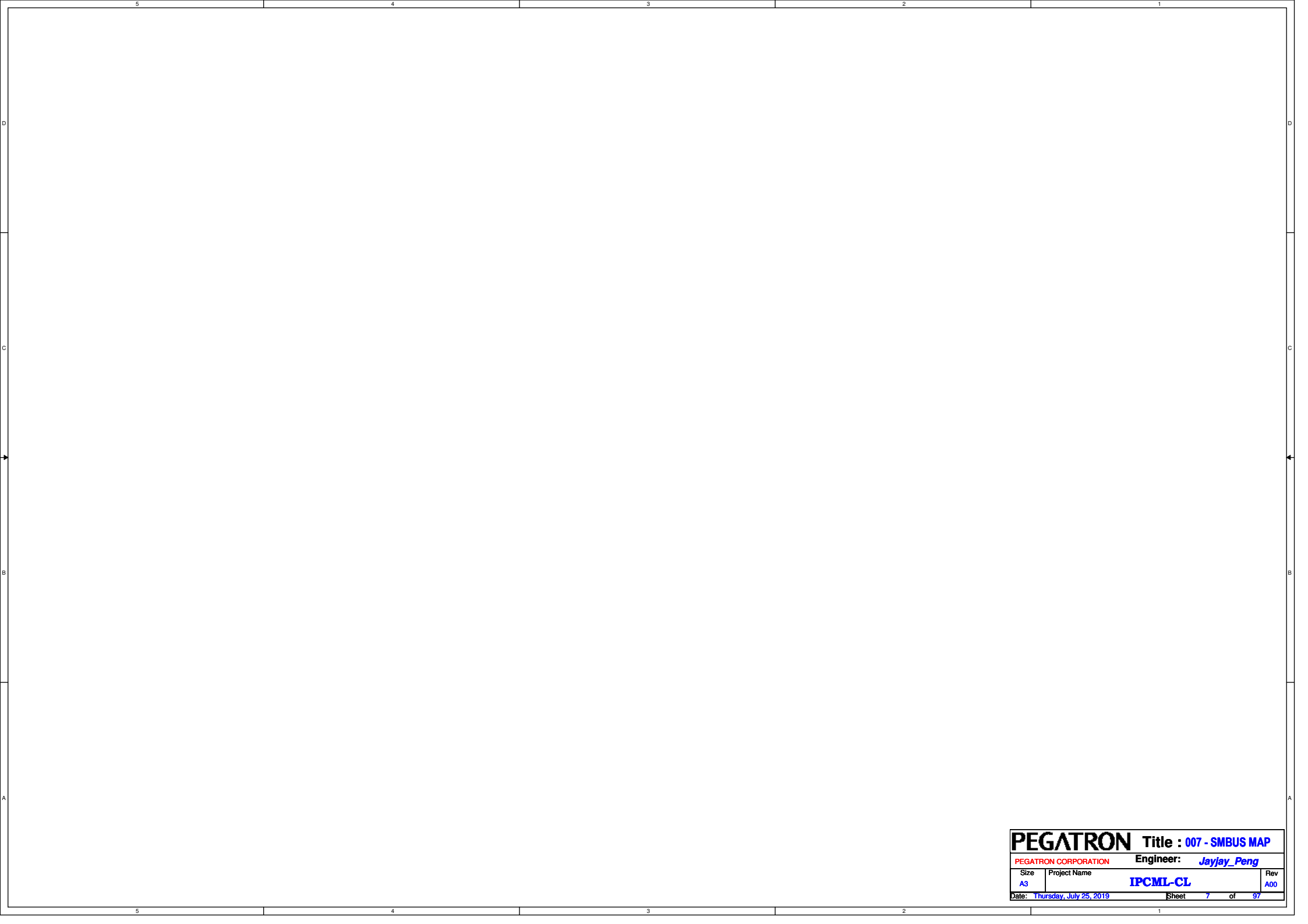
PEGATRON		Title : 004 - CLOCK DISTRIBUTION	
PEGATRON CORPORATION		Engineer: Jayjay Peng	
Size A3	Project Name IPCML-CL		Rev A00
Date: Thursday, July 25, 2019		Sheet 4 of 97	



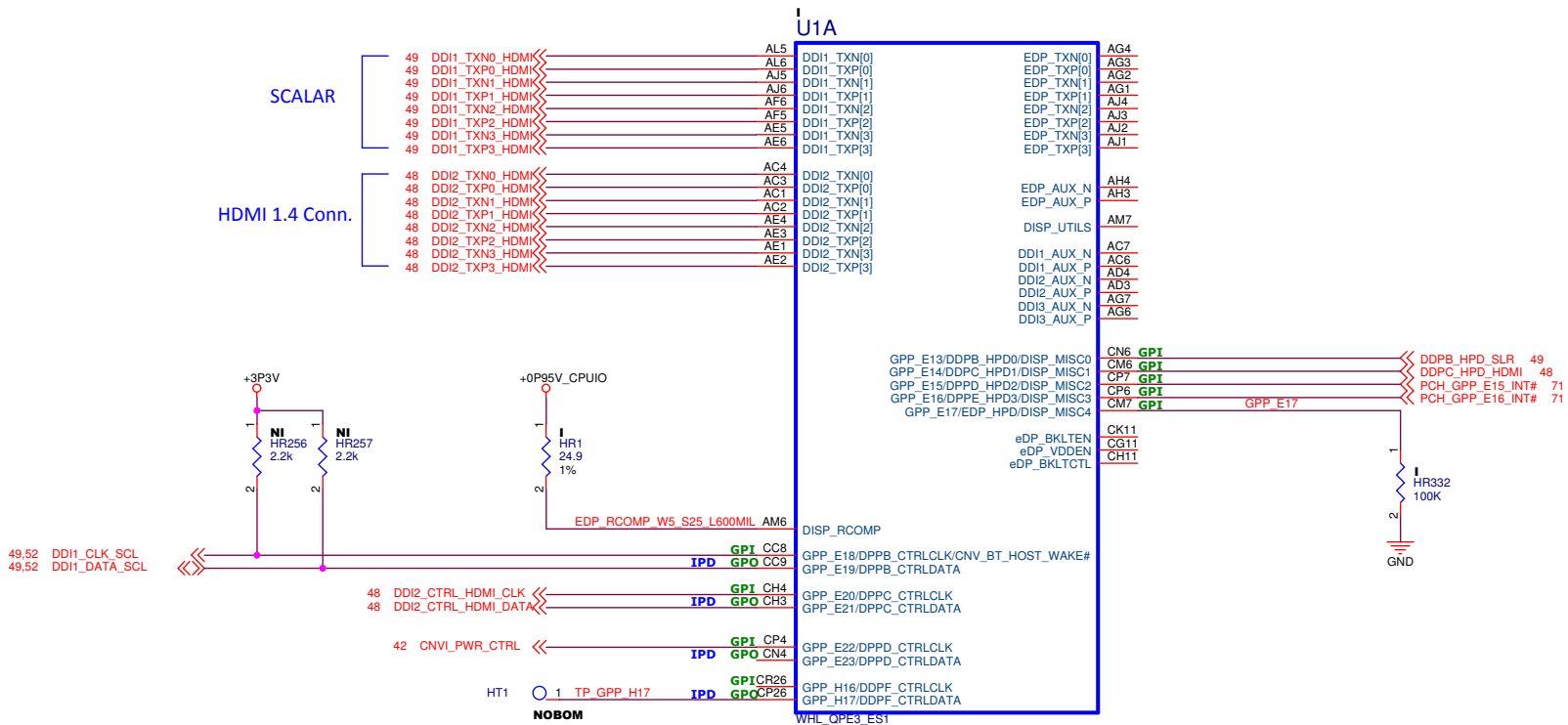
PEGATRON		Title : 005 - GPIO TABLE 1-2	
PEGATRON CORPORATION		Engineer: Jayjay Peng	
Size A3	Project Name IPCML-CL		Rev A00
Date: Thursday, July 25, 2019		Sheet 5 of 97	

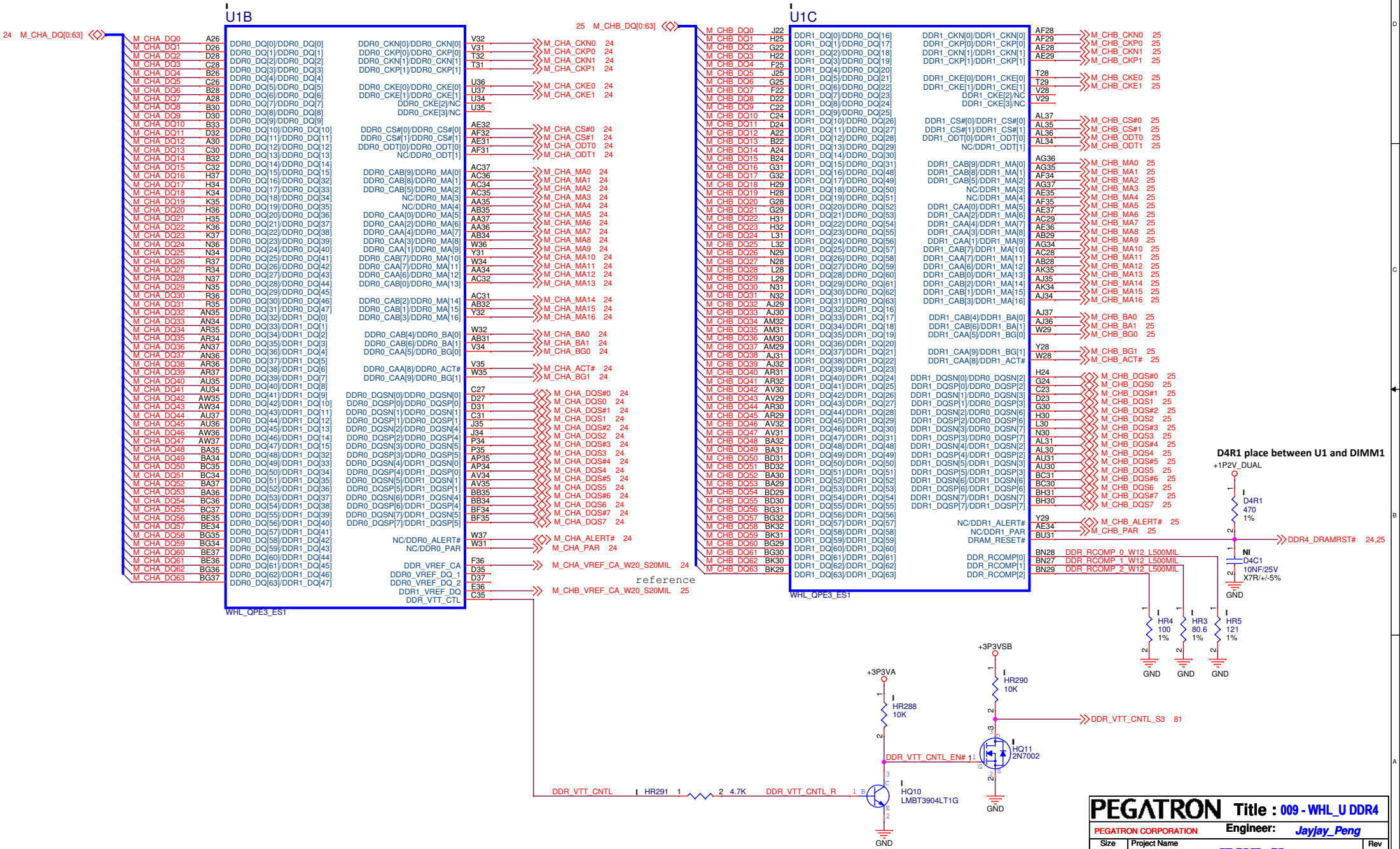


PEGATRON		Title : 006 - GPIO TABLE 2-3	
PEGATRON CORPORATION		Engineer: Jayjay_Peng	
Size	Project Name		Rev
A3	IPCML-CL		A00
Date: Thursday, July 25, 2019		Sheet	6 of 97

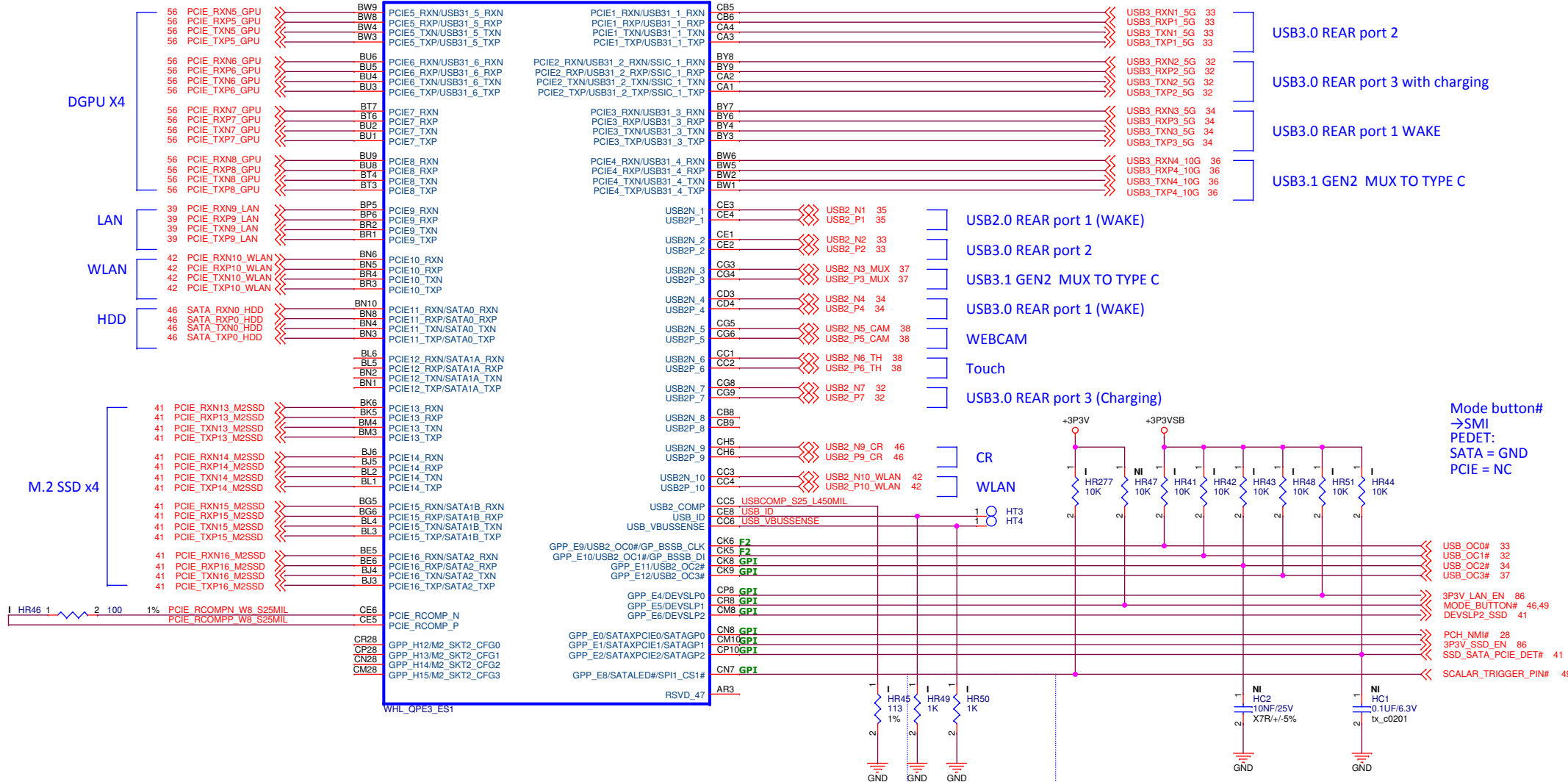


PEGATRON		Title : 007 - SMBUS MAP	
PEGATRON CORPORATION		Engineer: <i>Jayjay_Peng</i>	
Size A3	Project Name IPCML-CL		Rev A00
Date: <i>Thursday, July 25, 2019</i>		Sheet <i>7</i> of <i>97</i>	

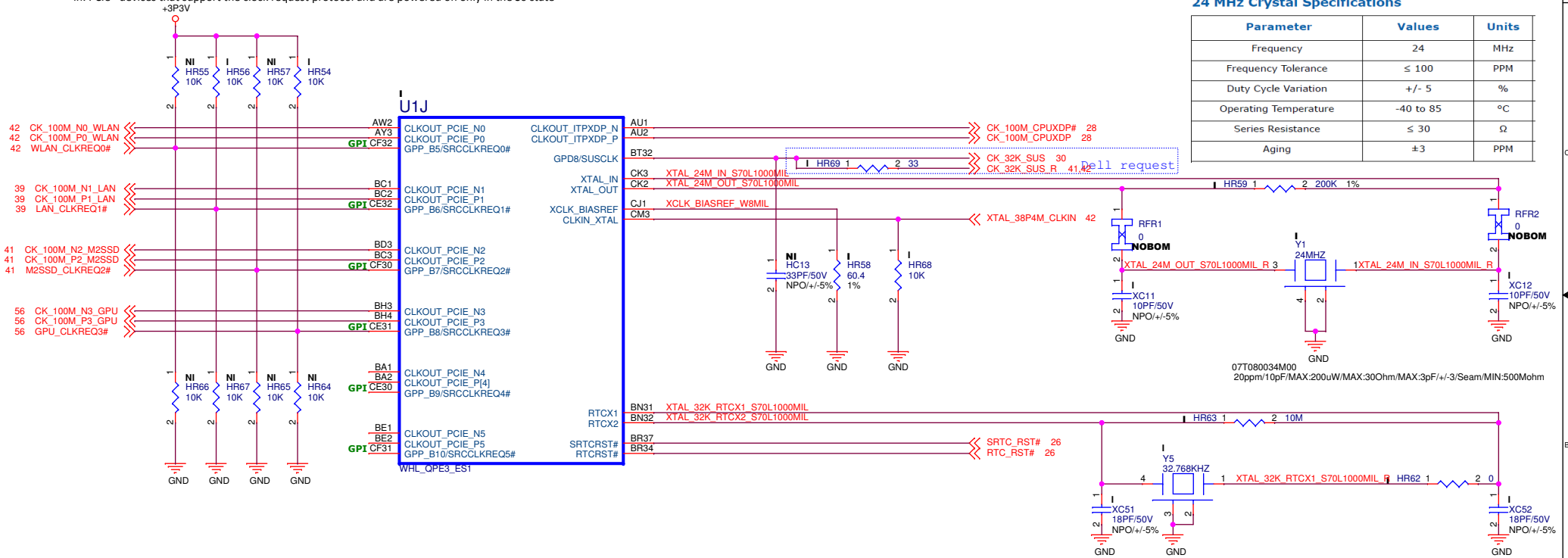




U1H



[Note]:
The corresponding SRCCLKREQ# pin resides
in. PCIe* devices that support the clock request protocol and are powered on only in the S0 state



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title 012 - WHL_U CLOCK	
Engineer: Jayjay_Peng	
Size A3	Project Name IPCML-CL
Date: Thursday, July 25, 2019	Sheet 12 of 97

CH32 GPIO ME DISABLE

+3P3VSB

HR74
10K

HDA_SDO:
1. Flash descriptor security:
Sampled Low: in effect.
Sampled High: override
2. HDA_SDO which sample high on
the rising edge of PWROK
Will also disable Intel ME.

ME_DISABLE#

HR75 1

ME_DISABLE# R

+3P3V

HR76
1K

Q6102 2

HR77 1

HR77 2

HR77 3

HR77 4

HR77 5

HR77 6

HR77 7

HR77 8

HR77 9

HR77 10

HR77 11

HR77 12

HR77 13

HR77 14

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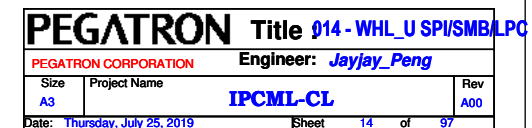
HR77 260

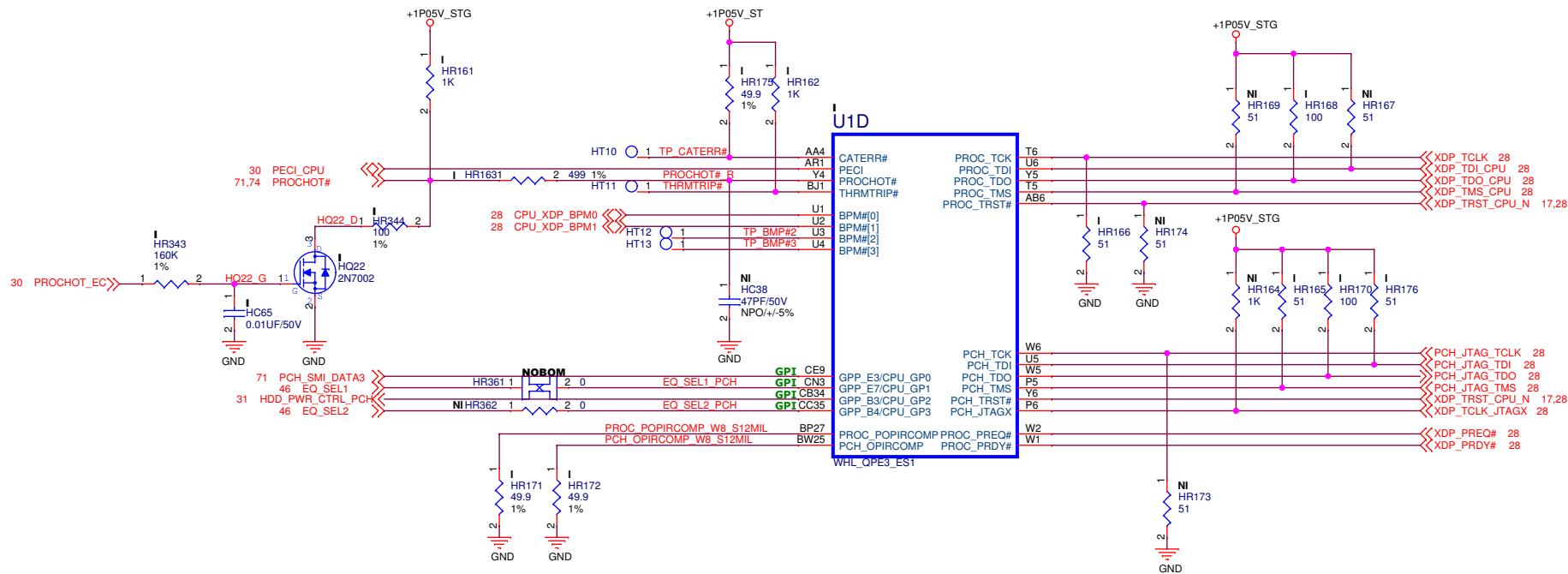
HR77 261

HR77 262

HR77 263

HR77 264





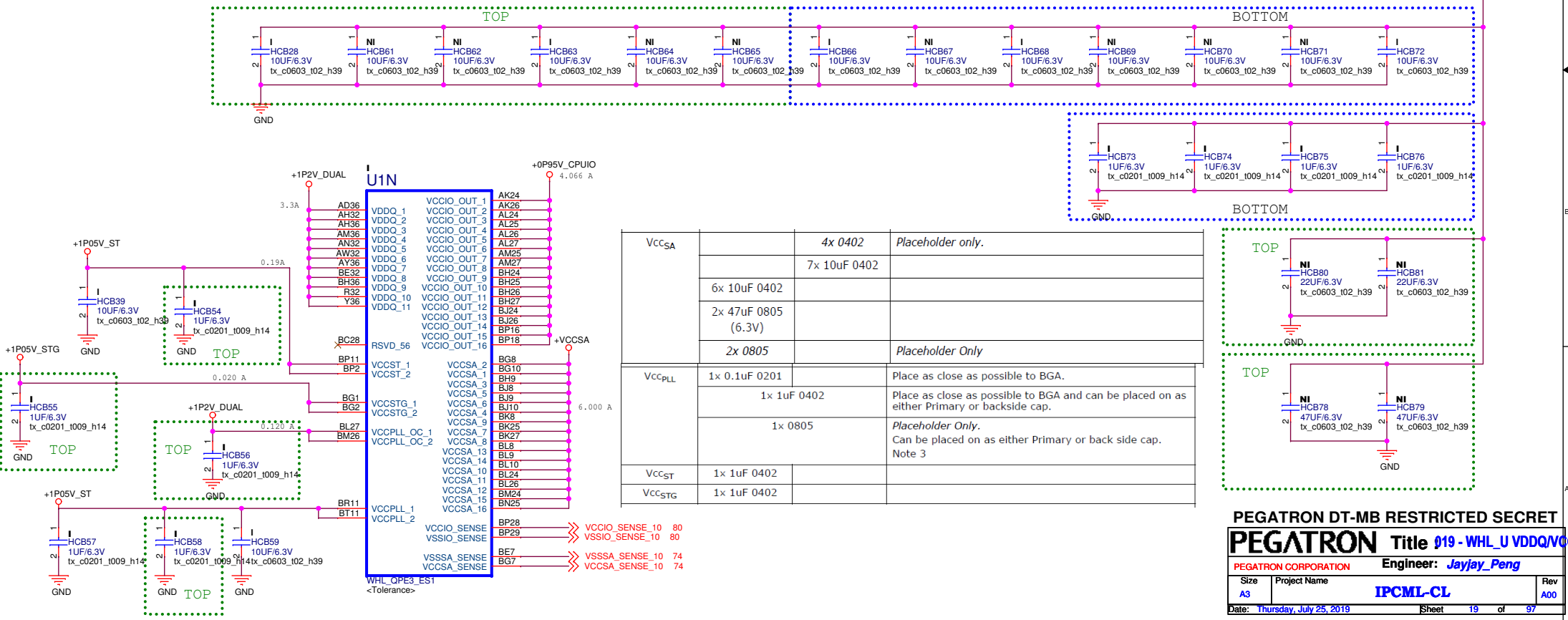
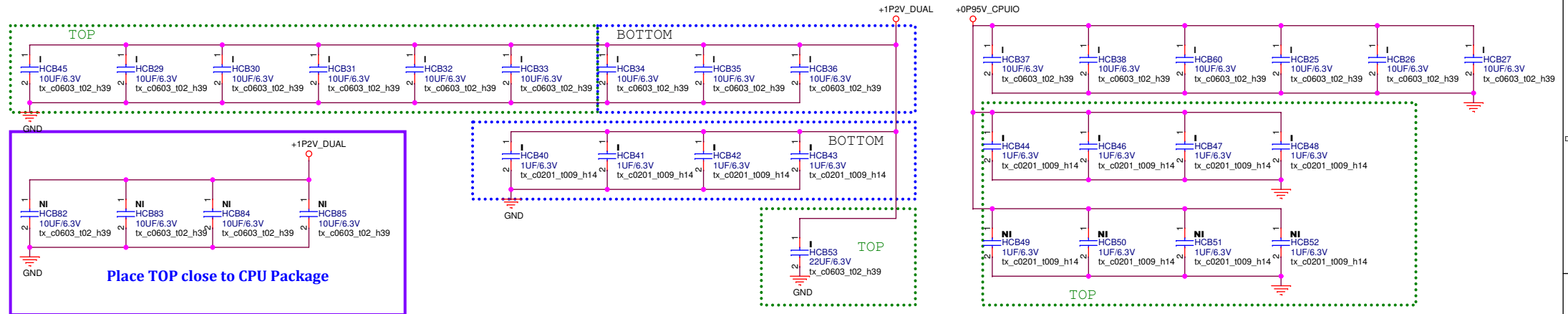
PEGATRON DT-MB RESTRICTED SECRET

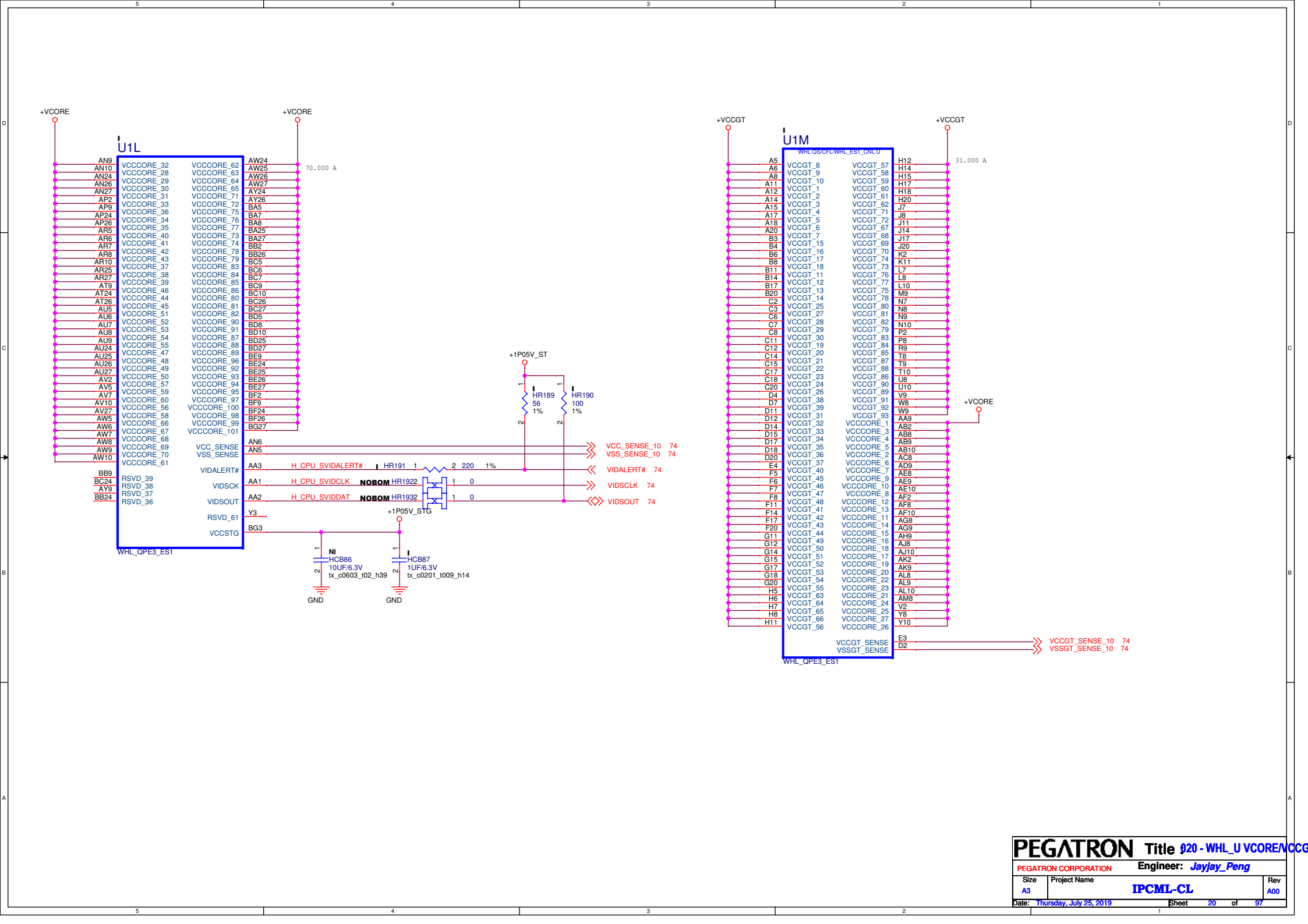
PEGATRON Title 917 - WHL_U MISC/JTAG/CLK

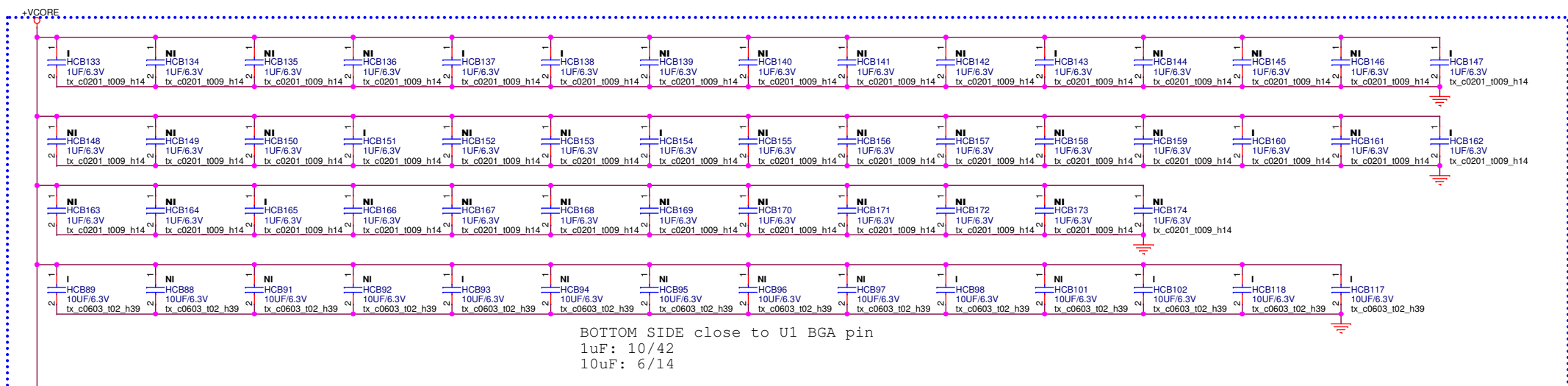
PEGATRON CORPORATION Engineer: Jayjay_Peng

Size A3	Project Name IPCML-CL	Rev A00
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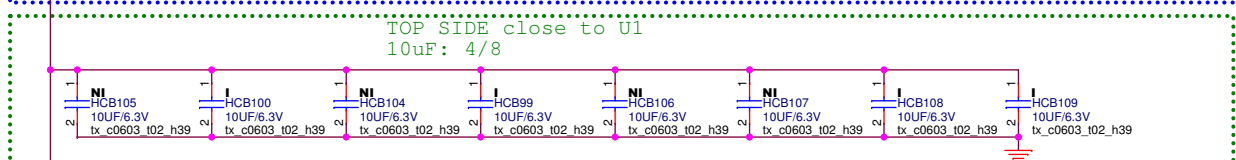
Date: Thursday, July 25, 2019 Sheet 17 of 97



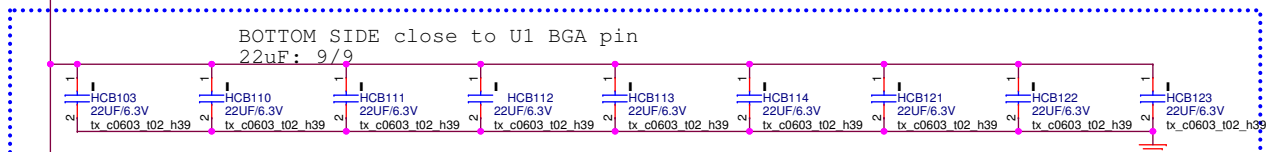




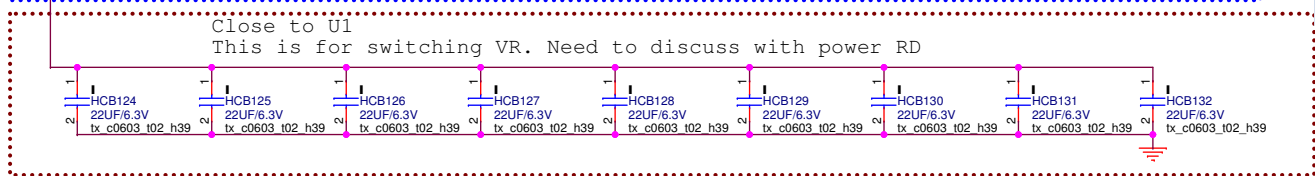
BOTTOM SIDE close to U1 BGA pin
1uF: 10/42
10uF: 6/14



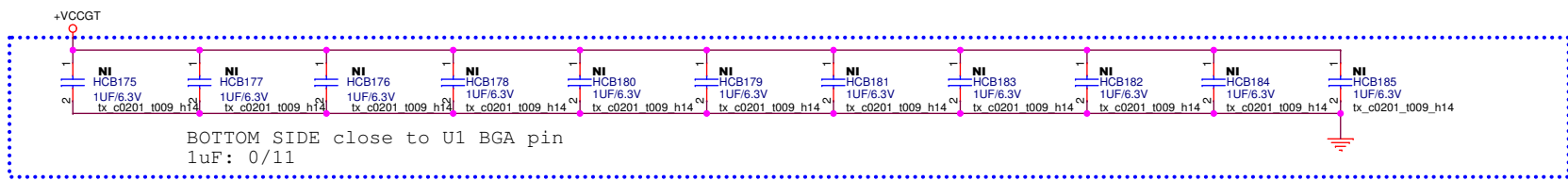
TOP SIDE close to U1
10uF: 4/8



BOTTOM SIDE close to U1 BGA pin
22uF: 9/9



Close to U1
This is for switching VR. Need to discuss with power RD



BOTTOM SIDE close to U1 BGA pin
1uF: 0/11

Domain	Primary Side cap	Secondary Side cap	Placement guideline
VCCORE		42x 1uF 0402/0201	To be placed as close as possible to the vias that connect to the BGA pins. Loadline for VCCORE is 1.8mOhm.
		14x 10uF 0402	
		9x 22uF 0603	
	8x 10uF 0402	18x 47uF 0805 (6.3V)	Place as close to the package as possible. Can be placed on as either Primary or back side cap.

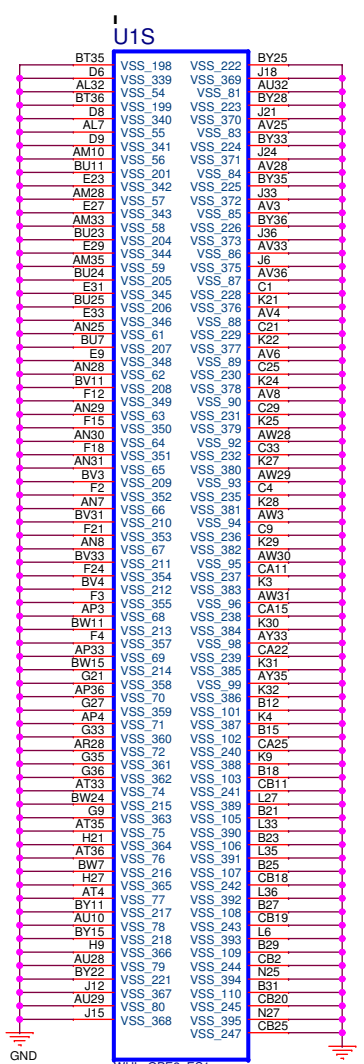
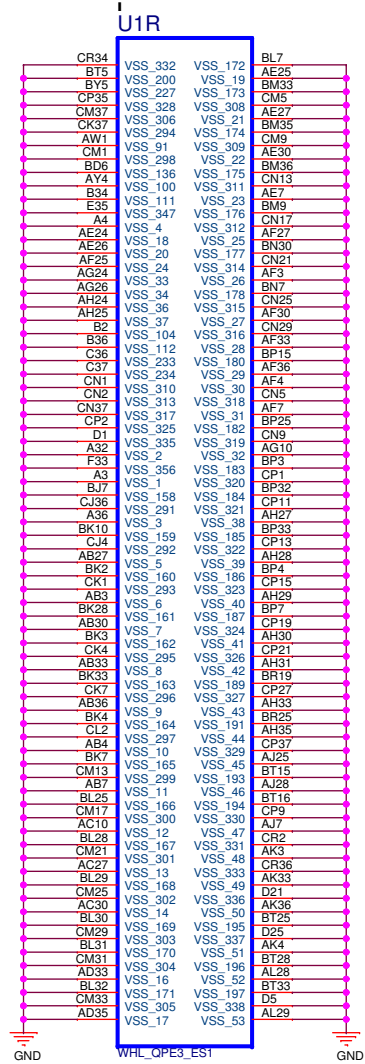


This is for switching VR. Need to discuss with power RD

VCCGT	15x 22uF 0603	Place as close to the package as possible
	4x 47uF 0805 (6.3V)	
	11x 1uF 0402/0201	Place as close to the package as possible
	15x 10uF 0402	

實際擺放10u+22u+47u總容值需與PDG一致 詳細數量需與POWER RD確認

DG:1UF→0201/0402,10UF→0402 ; NOW:1UF→0402 , 10UF→0603



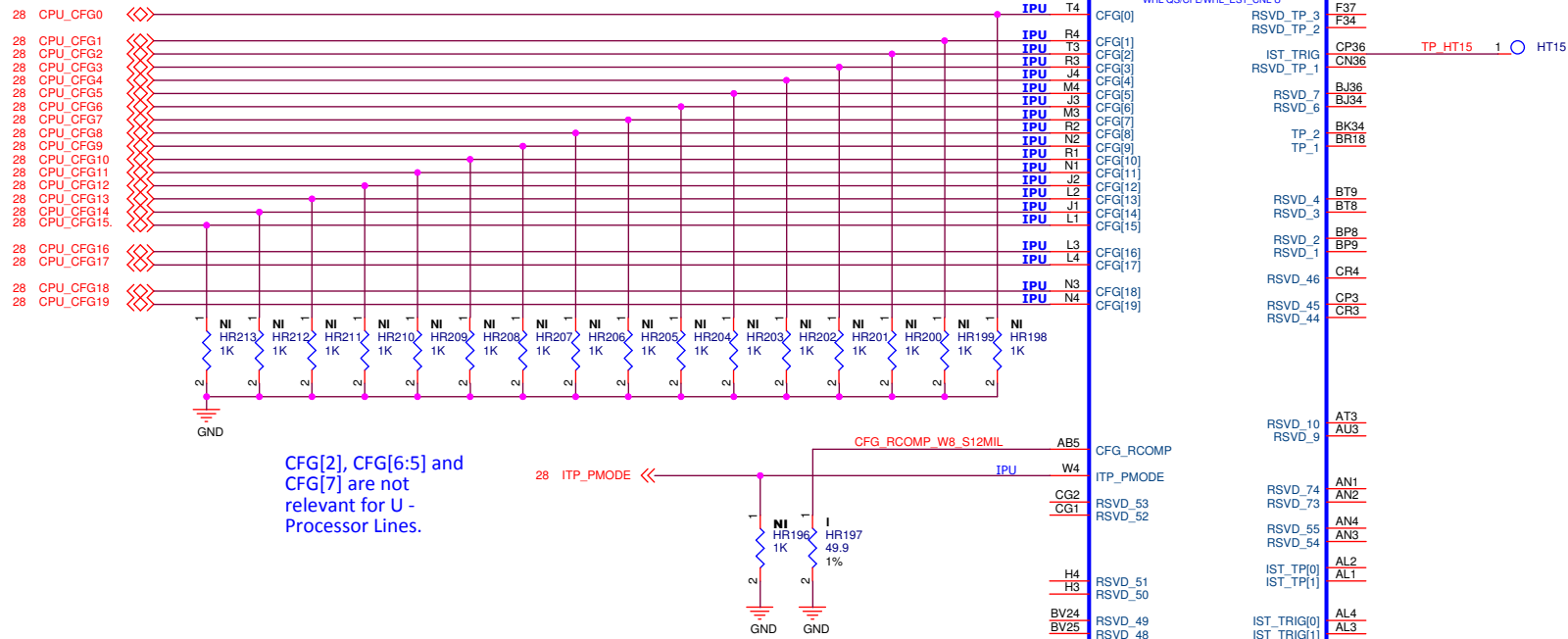
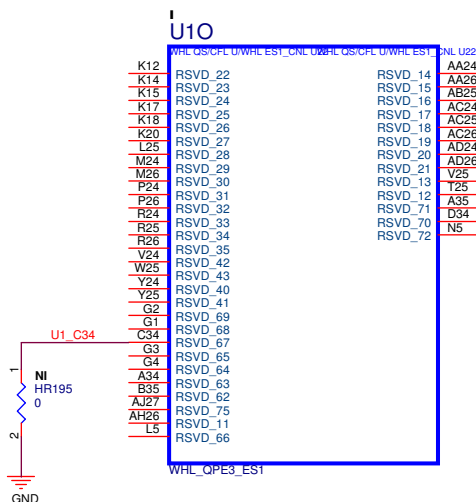


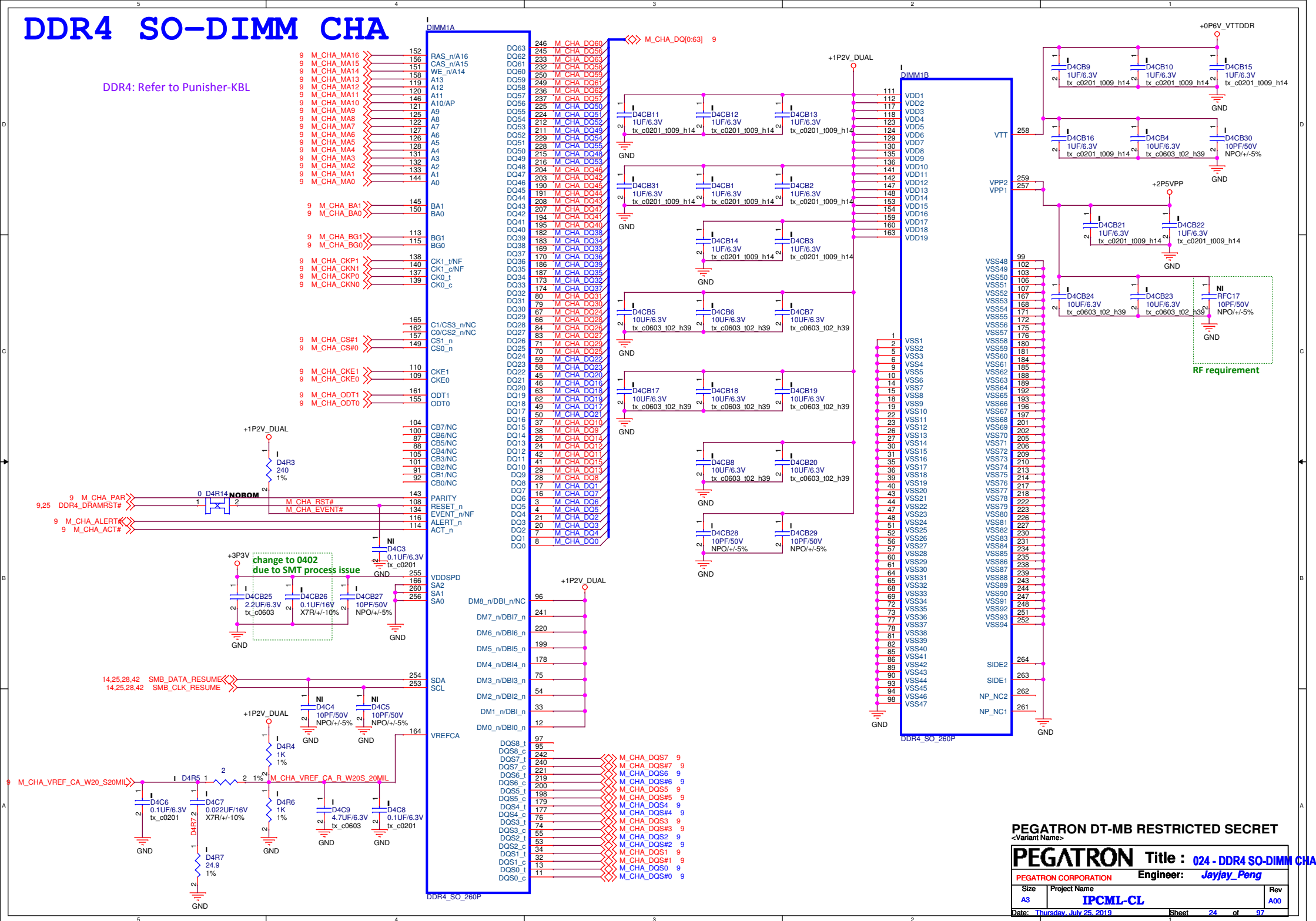
Table 1-43. Processor/PCH Strapping Checklist (Sheet 1 of 2)

Pin Name	Strap Description	Configuration (Default Value for Each Bit is 1 Unless Specified)	Default Value	✓
CFG[0]	Stall reset sequence after PCU PLL lock until de-asserted	Connect a series 1 KΩ resistor on the critical CFG[0] trace in a manner which does not introduce any stubs to CFG[0] trace. Route as needed from the opposite side of this series isolation resistor to the debug port. ITP will drive the net to GND.		
CFG[1]	Reserved. No connect			
CFG[2]	PCI Express* Static x16 Lane Numbering Reversal. A test point may be placed on the board for it.	1 = Normal operation 0 = Lane numbers reserved		
CFG[3]	Reserved configuration lane			
CFG[4]	Display Port Presence strap	1: Disabled - No Physical Display Port attached to Embedded DisplayPort*. No connect for disable. 0: Enabled - A Display Port device is connected to the Embedded Display Port. Pull-down to GND through a 1 KΩ ±5% resistor to enable port.	1	
CFG[6:5]	PCI Express* Bifurcation. A test point may be placed on the board for it.	00 = 1x8, 2x4 PCI Express* 01 = reserved 10 = 2x8 PCI Express* 11 = 1x16 PCI Express*		
CFG[7]	PEG Training. A test point may be placed on the board for them.	1 = (default) PEG train immediately following RESET# de assertion. 0 = PEG wait BIOS for training.	1	



DDR4 SO-DIMM CHA

DDR4: Refer to Punisher-KBL

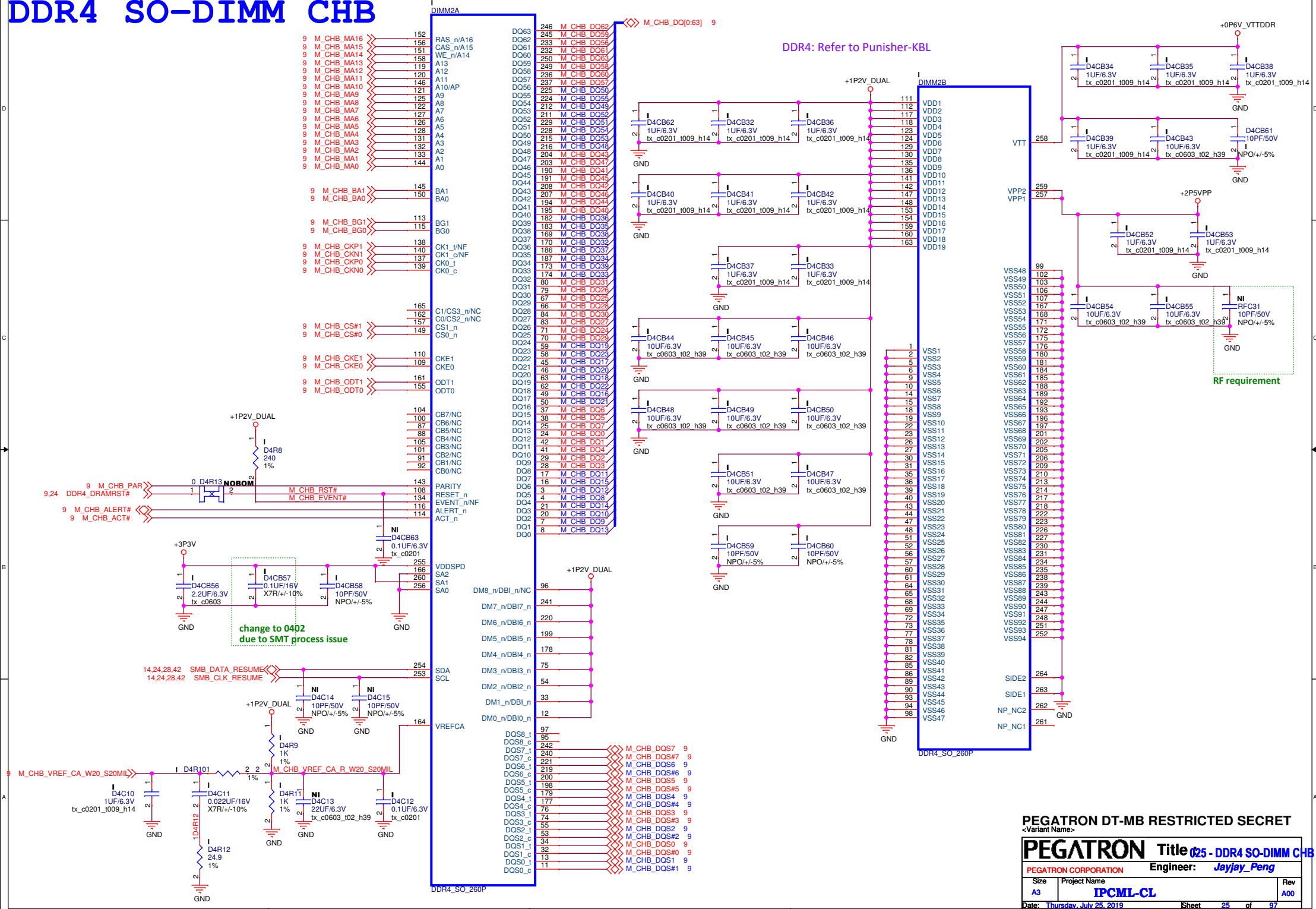


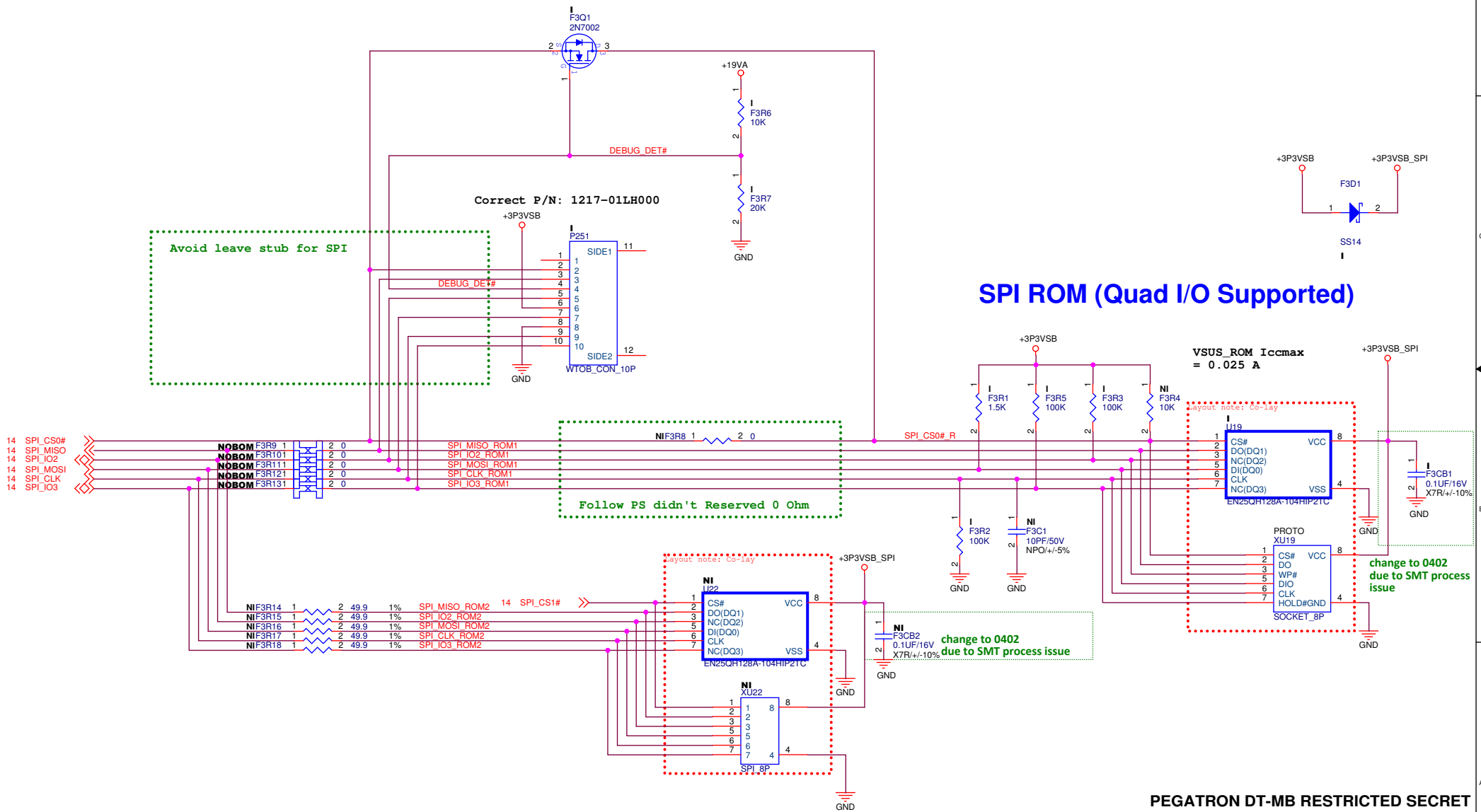
PEGATRON DT-MB RESTRICTED SECRET
-Variant Name-

PEGATRON Title : 024 - DDR4 SO-DIMM CHA
PEGATRON CORPORATION Engineer: Jayjay_Peng

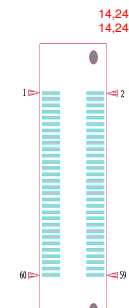
Size	Project Name	Rev
A3	IPCML-CL	A00
Date: Thursday, July 25, 2019 Sheet 24 of 97		

DDR4 SO-DIMM CHB

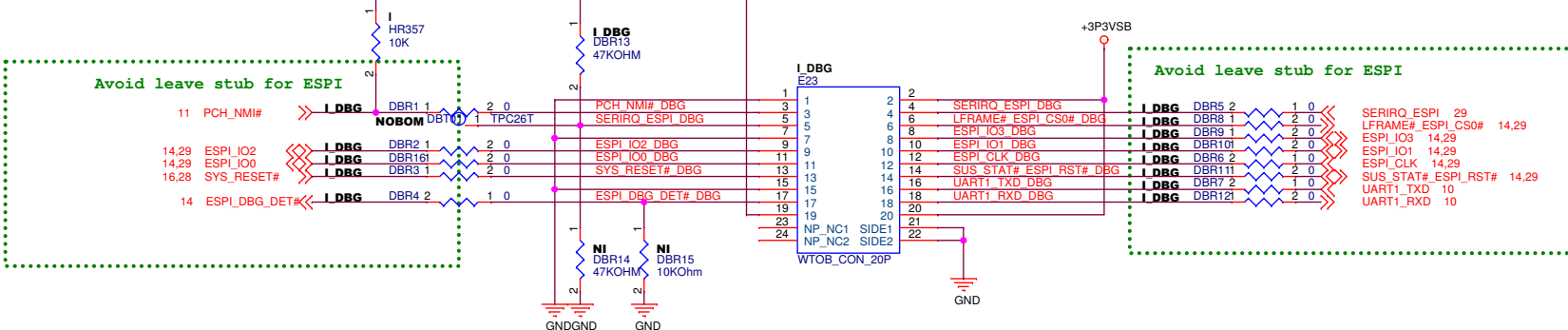




The schematic diagram illustrates the power supply circuit for the Proto E25 board. A +1P05VSB input is connected to a network of capacitors (HC42, 0.1uF/6.3V, tx_c0201) and a diode (NI HR225) to ground. The output of this network is connected to the VCC_OBS_AB and VCC_OBS_CD pins of the Proto E25 board.



BOTTOM SIDE VIEW
HRS/DF9C-31S-1V(22)^{EW}
PCB FOOTPRINT



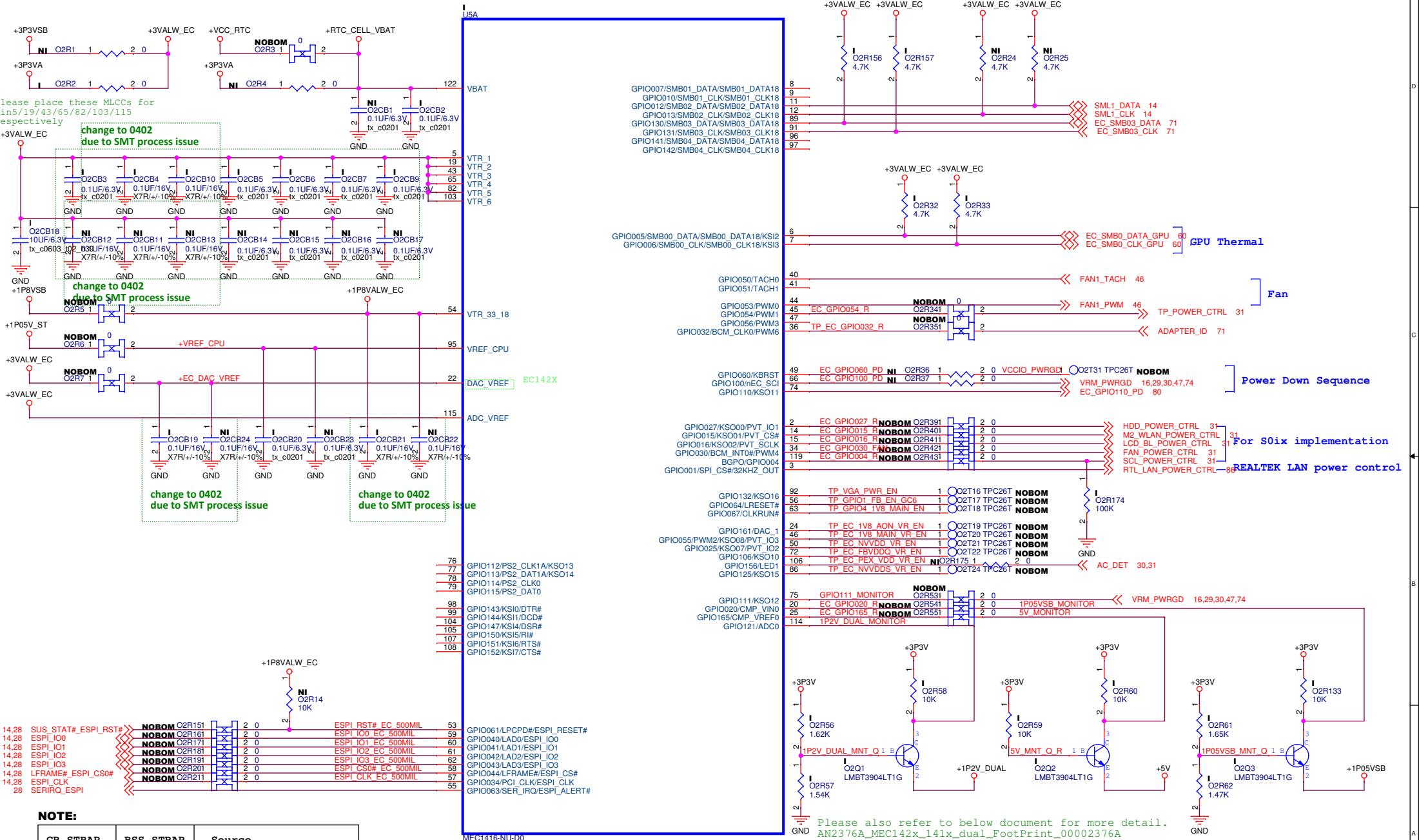
PFGATRON Title : 028 - XDP/ESPI DEBUG

Engineer:

Size	Project Name	Revised By
A3	IPCML-CL	AC

Date: Thursday, July 25, 2019 Sheet 28 of 97

NOTE:
3.3V/1.8V Operation Only and DO NOT exceed 5V



NOTE:

CR_STRAP	BSS_STRAP	Source
0	X	Use 3.3V Private SPI
1	0	Use eSPI Flash Channel
	1	Use 3.3V Shared SPI

If the eSPI Flash Channel is used for booting, the GPIO123/SHD_CS# pin must be used as RSMRST#. This pin will be driven high by the boot ROM code in order to activate the eSPI flash channel. If the SHD_SPI port is used for booting, then any unused GPIO may be used for RSMRST#.

NOTE: Colay EC141X & EC142X on the POC CKT

	PIN22	PIN31	PIN51	PIN81
EC141X	DAC_VREF	SHD_IO3	VSS	UART_TX
EC142X	GPIO066	DPWROK	GPIO167	VL_STRAP

PEGATRON DT-MB RESTRICTED SECRET

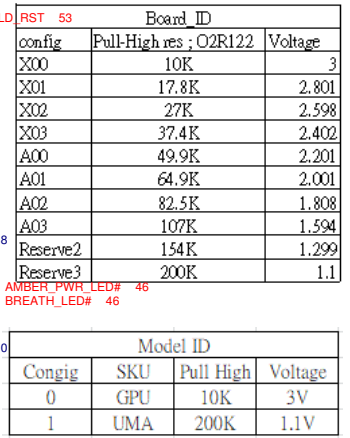
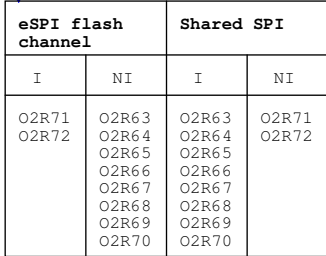
PEGATRON Title 929 - MICROCHIP MEC1416

PEGATRON CORPORATION Engineer: Jayjay_Peng

Size A3	Project Name IPCML-CL	Rev A00
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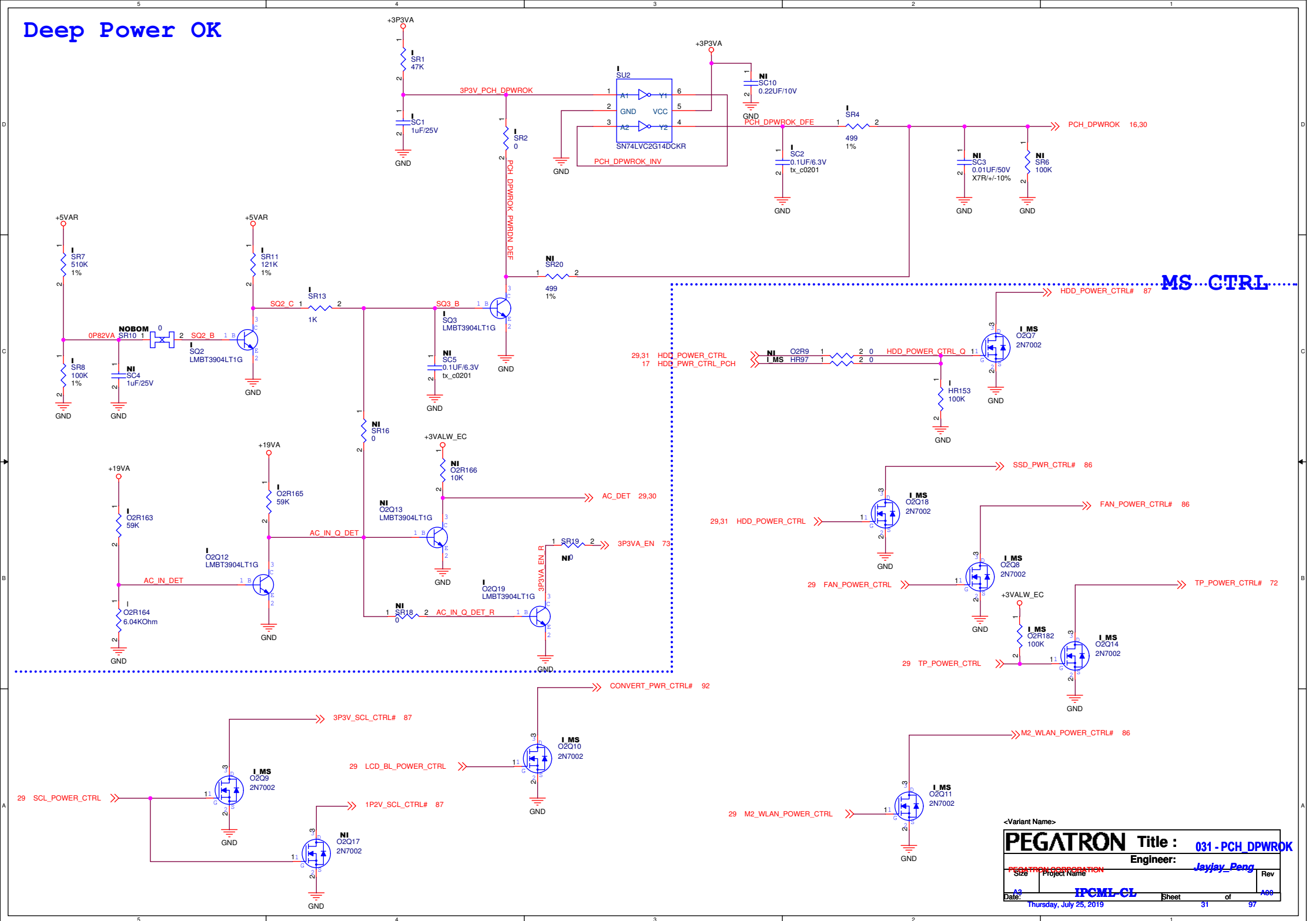
Date: Thursday, July 25, 2019 Sheet 29 of 97

PRIM_PWRGD High以後 EC會先LOAD BIOS ROM 的CODE
等Code load 完成在發RSMRST

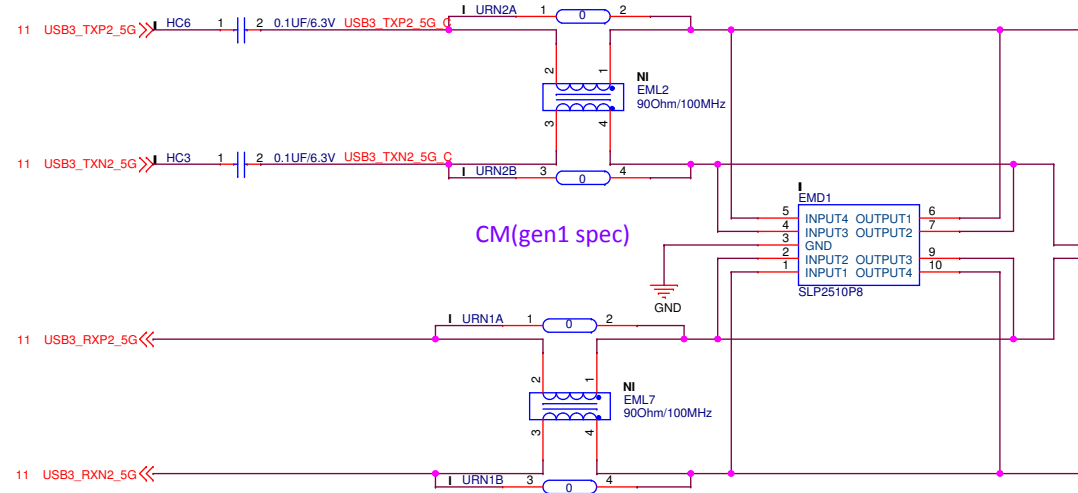


PEGATRON DT-MB RESTRICTED SECRET			
PEGATRON		Title :	030 - MICROCHIP MEC 416
PEGATRON CORPORATION		Engineer:	Jayjay_Peng
Size A3	Project Name IPCML-CL	Rev A00	
Date: Thursday, July 25, 2019		Sheet	30 of 97

Deep Power OK



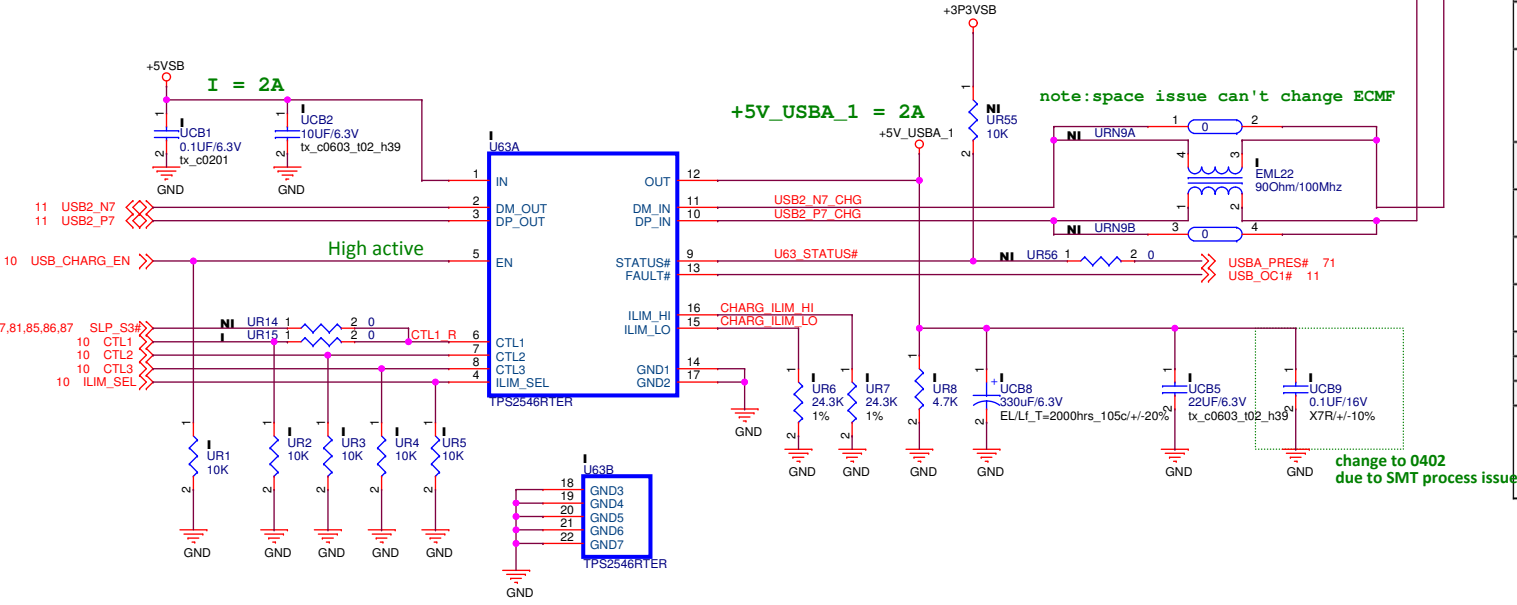
USB3.0 REAR port 3 with charging



CM(gen1 spec)

$$I_{OS_typ} (mA) = \frac{50,500}{(R_{ILIM_XX} (k\Omega) + 0.1)}$$

Current limit: 24K 1%
when:
23.76K Ohm:2116mA
24.24K Ohm:2075mA



USB3_TXP2_5G_CMC
USB3_TXN2_5G_CMC
USB3_RXP2_5G_CMC
USB3_RXN2_5G_CMC

CTL1	CTL2	CTL3	ILIM_SEL	Mode	Current Limit Setting	STATUS Output (Active low)	Comment
0	0	0	0	Discharge	NA	OFF	OUT held low
0	0	0	1	Discharge	NA	OFF	
0	0	1	0	DCP_Auto	ILIM_HI	OFF	Data Lines Disconnected
0	0	1	1	DCP_Auto	IOS_PW & ILIM_HI (1)	DCP load present (2)	Data Lines Disconnected and Power Wake Function Active
0	1	0	0	SDP	ILIM_LO	OFF	Data Lines Disconnected
0	1	0	1	SDP	ILIM_HI	OFF	Data Lines connected
0	1	1	0	DCP_Auto	ILIM_HI	OFF	Data Lines Disconnected
0	1	1	1	DCP_Auto	ILIM_HI	DCP load present (3)	Data Lines Disconnected and Port Power Mgt. Function Active
1	0	0	0	DCP Forced Shorted	ILIM_LO	OFF	Device Forced to stay in DCP BC
1	0	0	1	DCP Forced Shorted	ILIM_HI	OFF	1.2 charging mode
1	0	1	0	DCP / Divider1	ILIM_LO	OFF	Device Forced to stay in DCP
1	0	1	1	DCP / Divider1	ILIM_HI	OFF	Divider 1 Charging Mode
1	1	0	0	SDP	ILIM_LO	OFF	Data Lines Connected
1	1	0	1	SDP	ILIM_HI	OFF	
1	1	1	0	SDP (4)	ILIM_LO	OFF	
1	1	1	1	CDP (4)	ILIM_HI	CDP load present (5)	Data Lines Connected and Port Power Mgt. Function Active

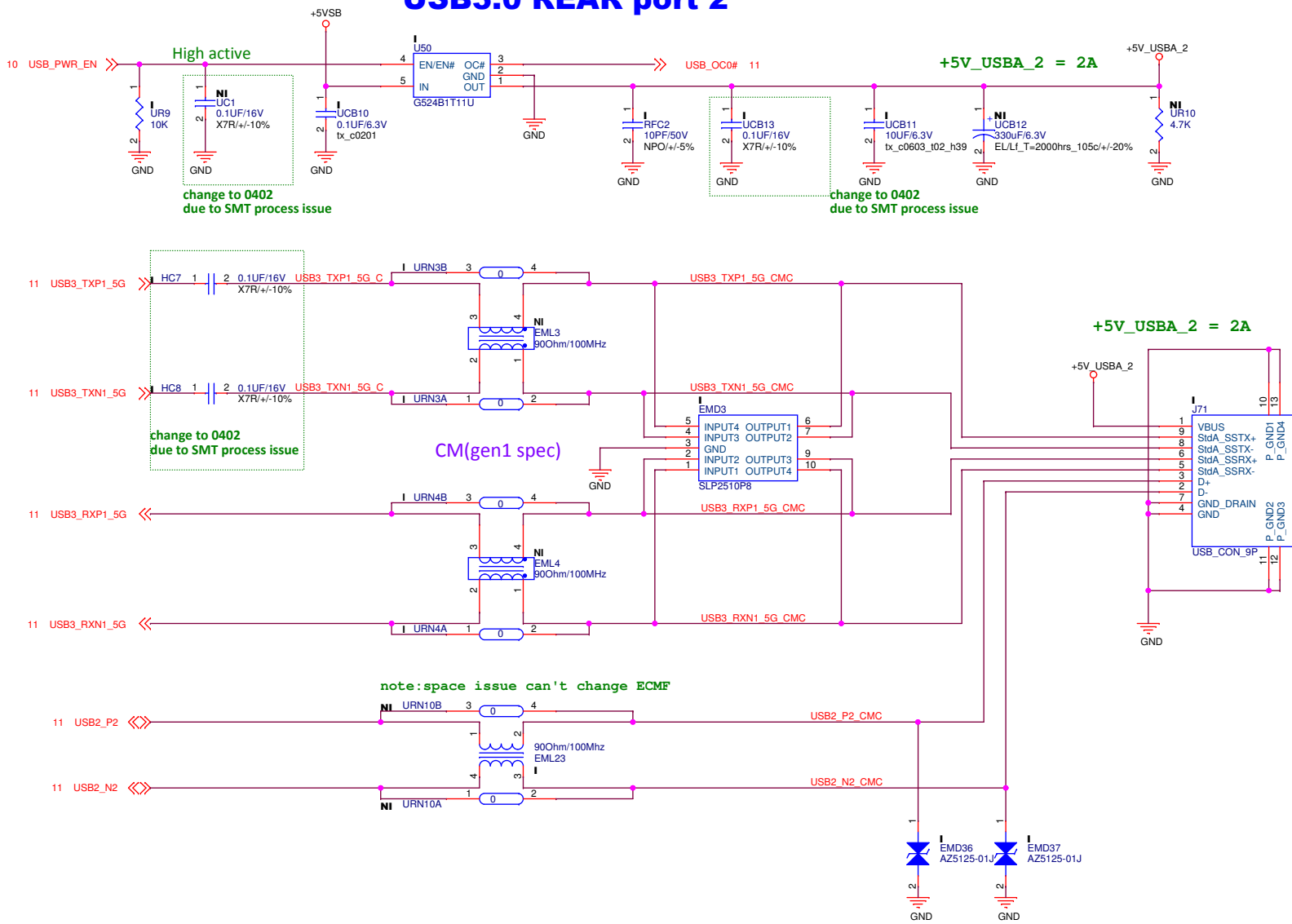
Pin Number	Signal ASSIGNMENT
PIN 1	VBUS
PIN 2	D-
PIN 3	D+
PIN 4	GND
PIN 5	StdA_SSRX-
PIN 6	StdA_SSRX+
PIN 7	GND_DRAIN
PIN 8	StdA_SSTX-
PIN 9	StdA_SSTX+

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : 032 - USB 3.0 CHARGING PORT

Size	Project Name	Rev
A3	IPCML-CL	A00
Date:	Thursday, July 25, 2019	Sheet 32 of 97

USB3.0 REAR port 2



<Variant Name>

PEGATRON Title : 033 - USB 3.0 PORT

PEGATRON CORPORATION

Engineer: Jayjay_Peng

Size A3

Project Name

IPCML-CL

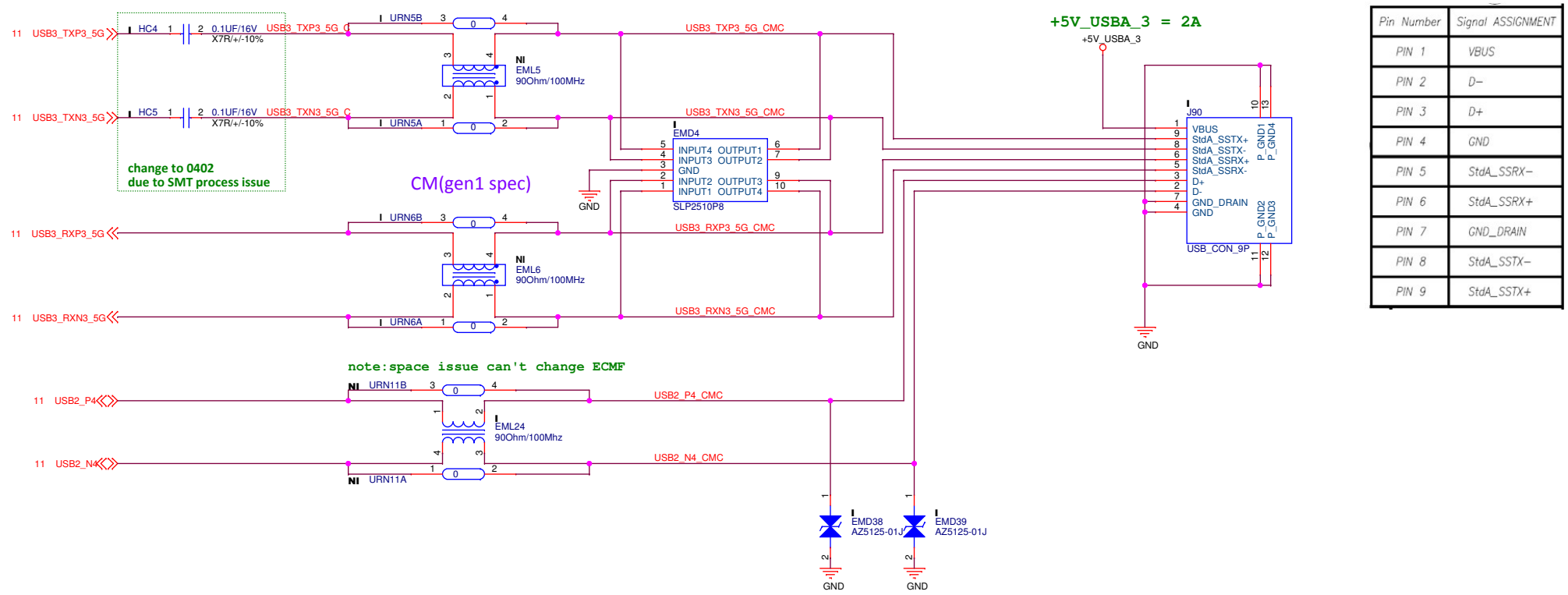
Date: Thursday, July 25, 2019

Sheet 33 of 97

Rev

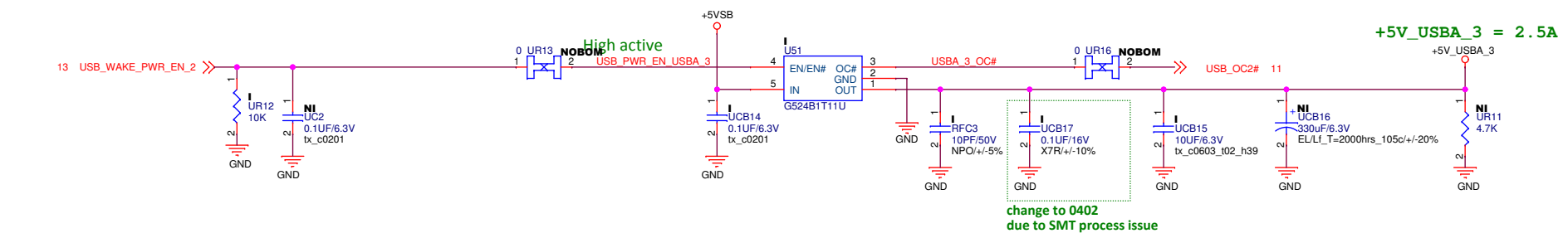
A00

USB3.0 REAR port 1(WAKE)



Pin Number	Signal ASSIGNMENT
PIN 1	VBUS
PIN 2	D-
PIN 3	D+
PIN 4	GND
PIN 5	StdA_SSRX-
PIN 6	StdA_SSRX+
PIN 7	GND_DRAIN
PIN 8	StdA_SSTX-
PIN 9	StdA_SSTX+

+5V_USBA_3 = 2A

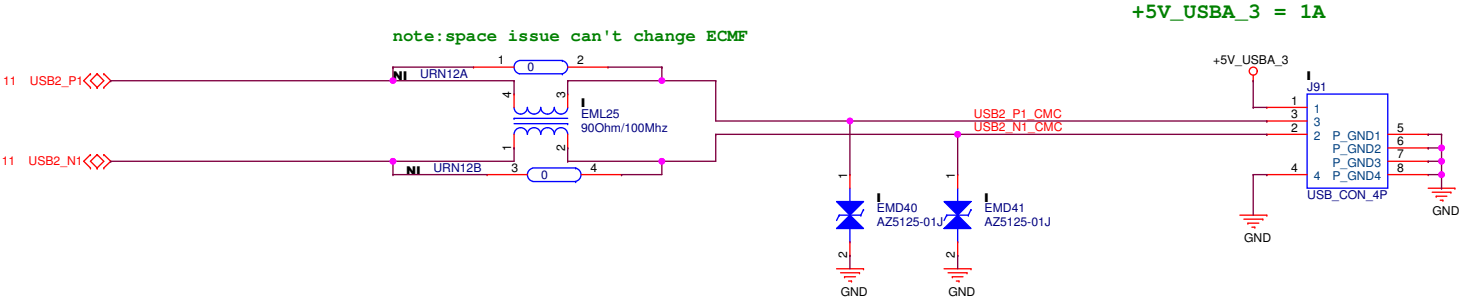


+5V_USBA_3 = 2.5A

<Variant Name>

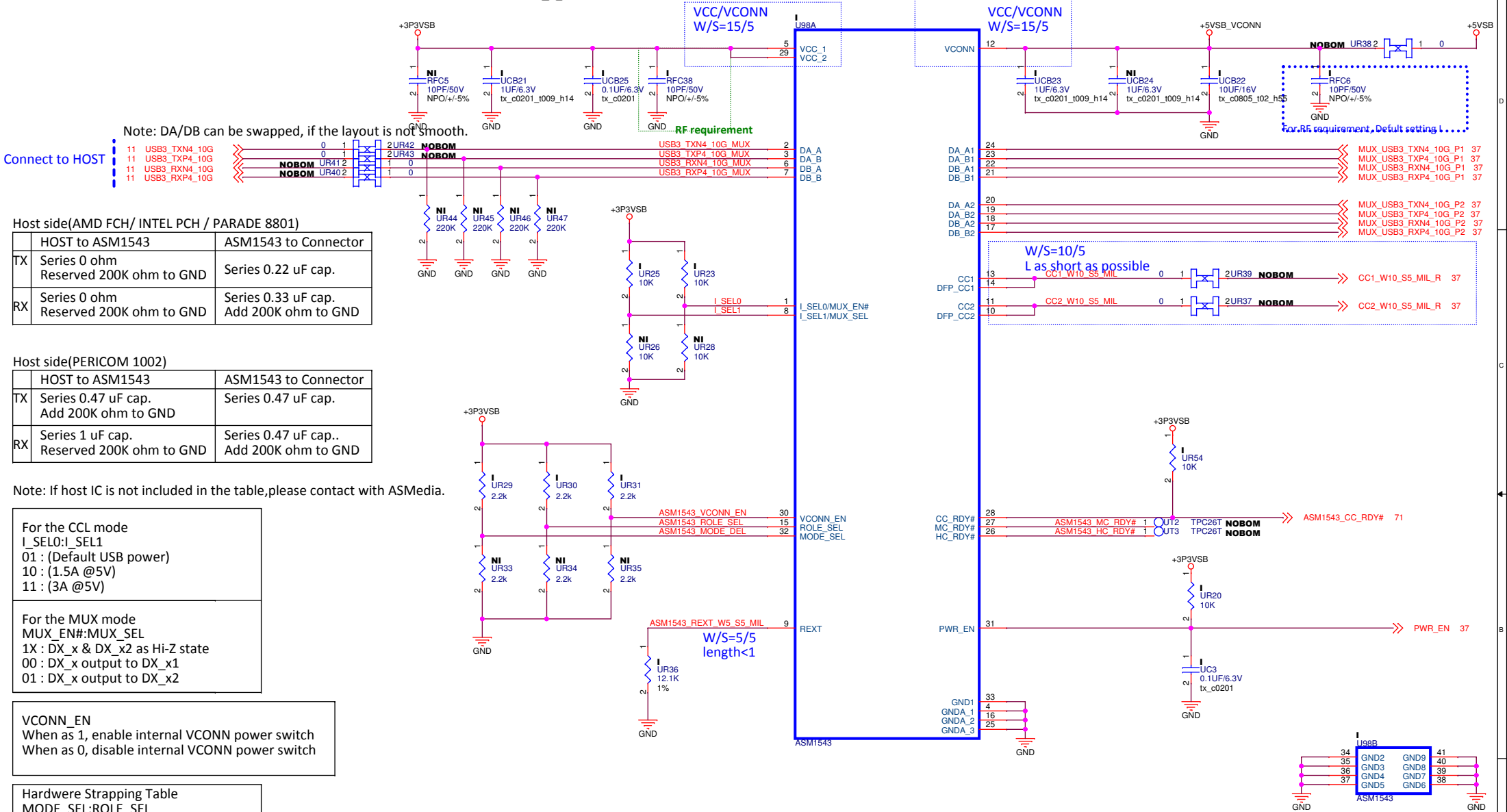
PEGATRON		Title : 034 - USB 3.0 PORT	
PEGATRON CORPORATION		Engineer: Jayjay_Peng	
Size A3	Project Name	IPCML-CL	
Date: Thursday, July 25, 2019	Sheet 34	of 97	

USB2.0 REAR port1(WAKE)

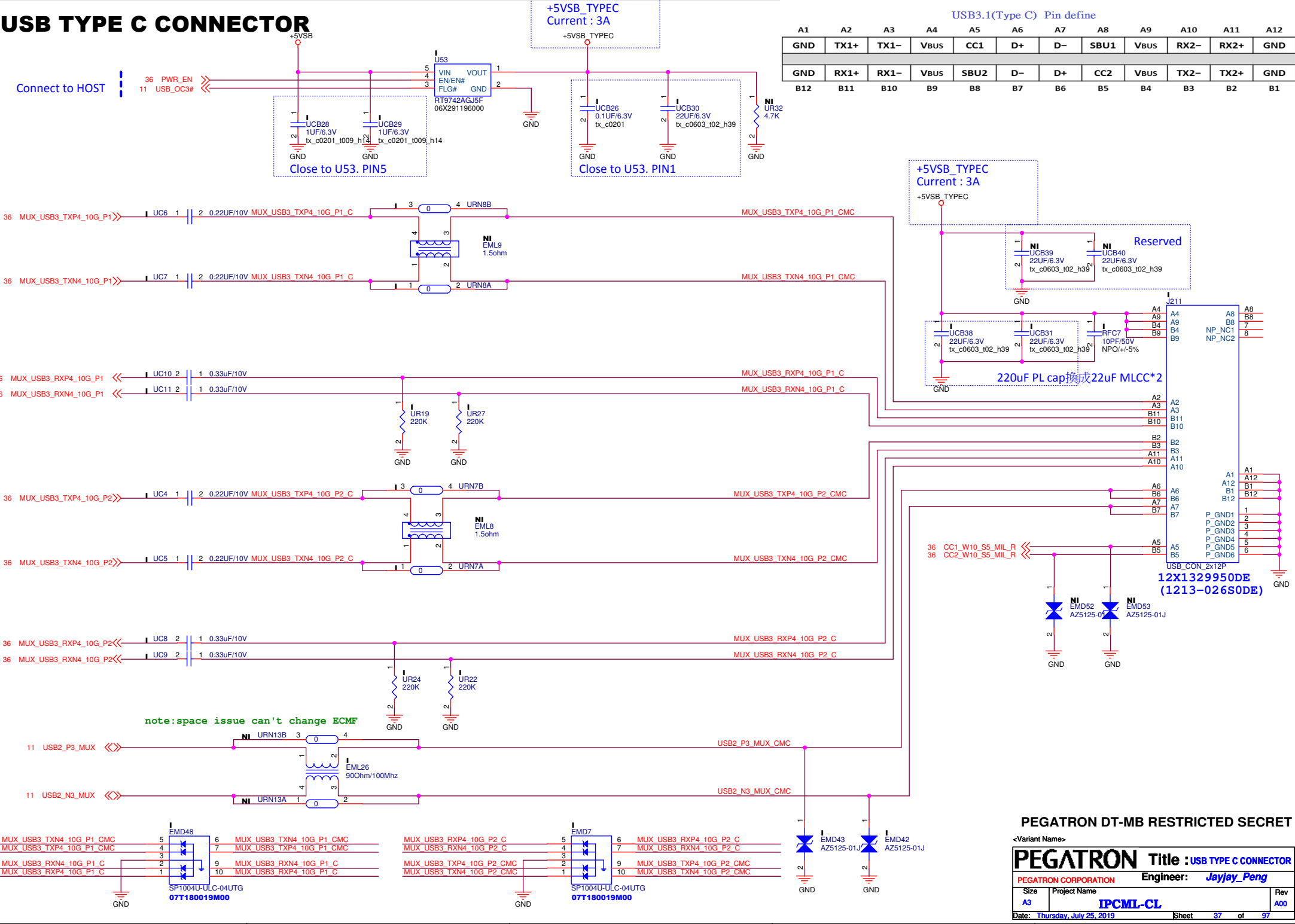


Pin	Name	Description
1	VCC	+5 VCC
2	D-	Data -
3	D+	Data +
4	GND	Ground

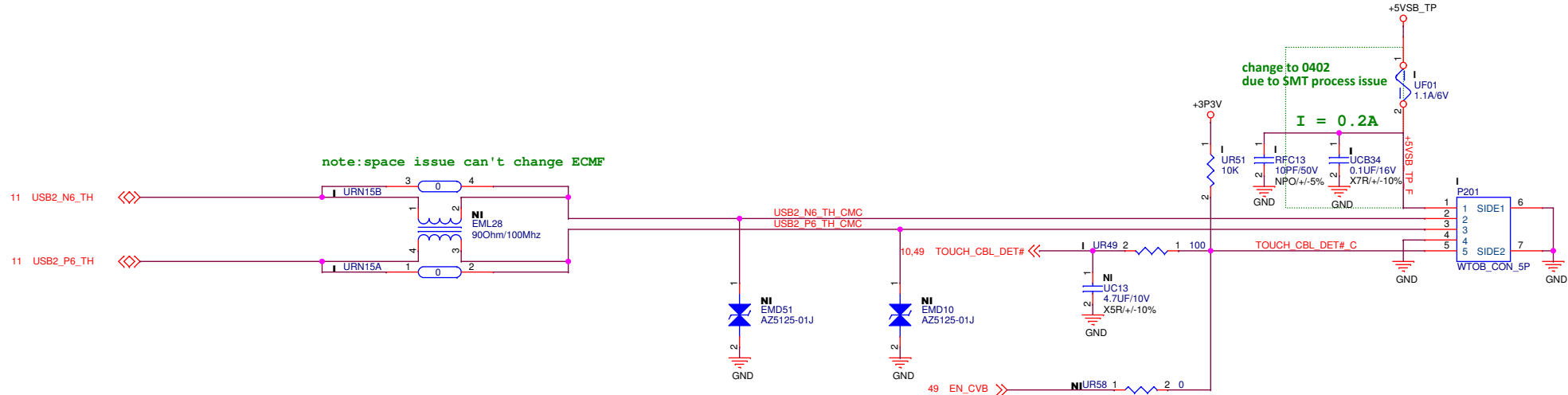
USB3.1 GEN2 TYPE C MUX ASM1543 for Type-C current mode



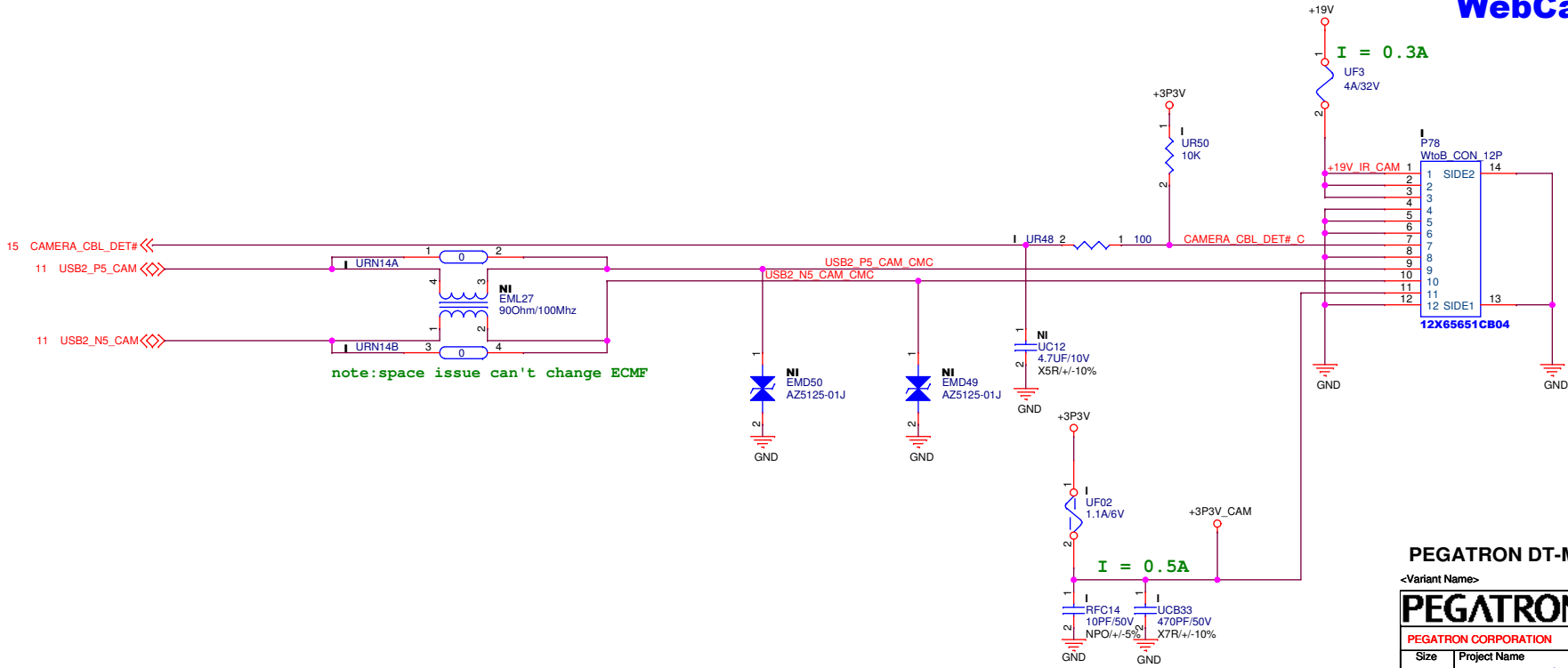
USB TYPE C CONNECTOR



Touch Panel

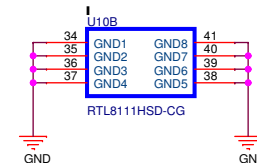
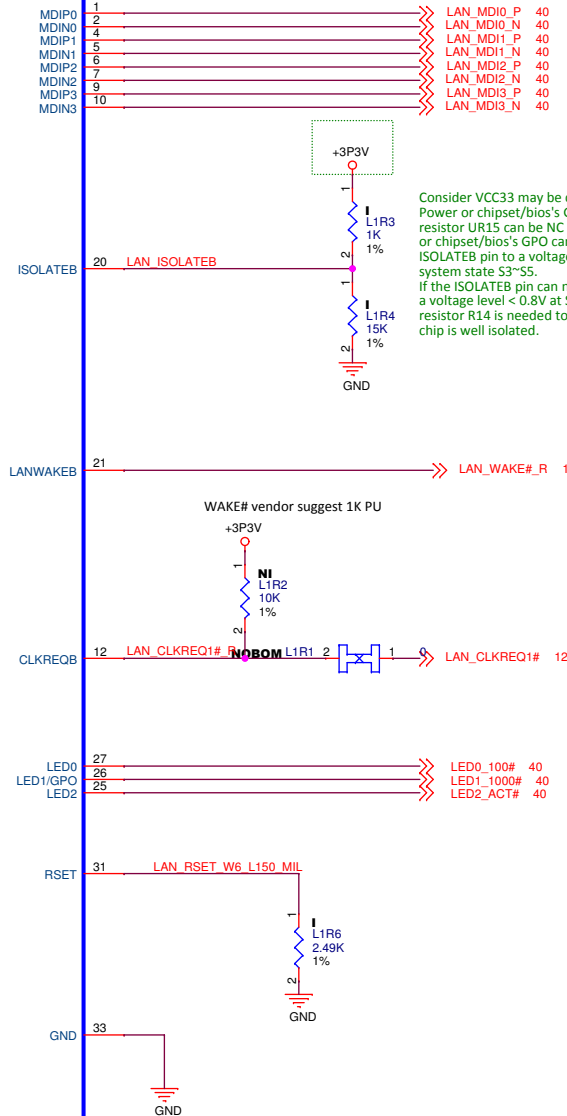
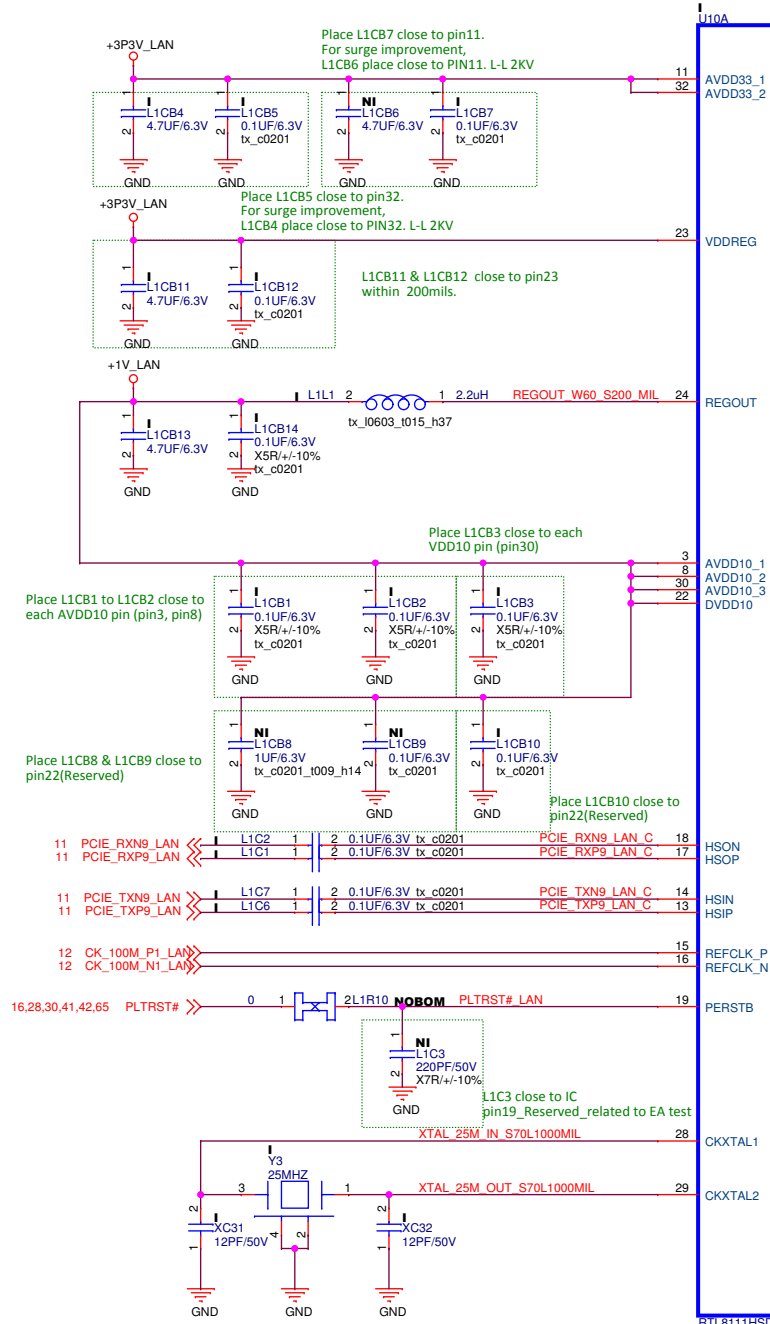


WebCam



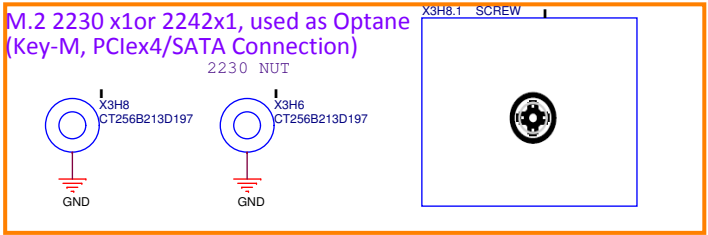
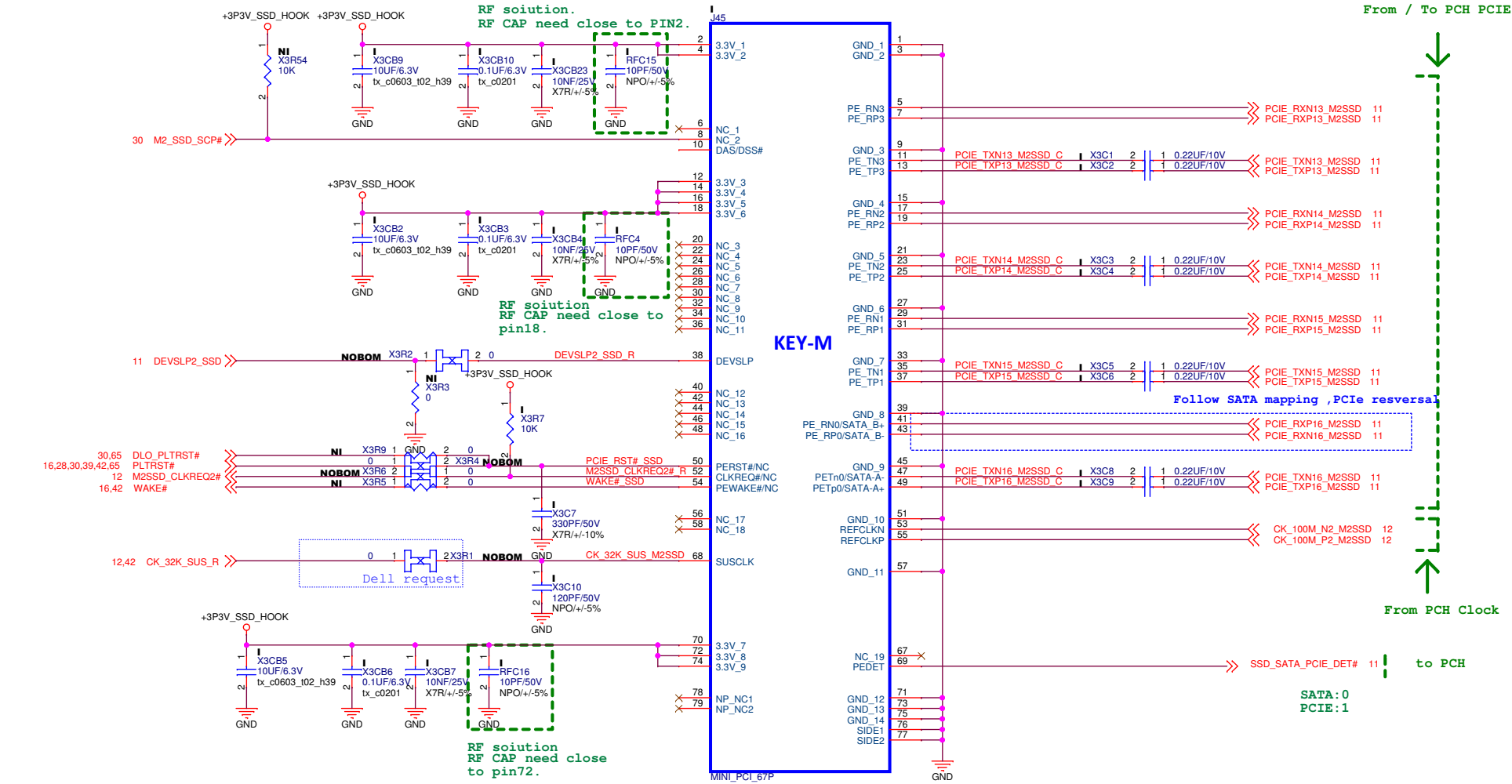
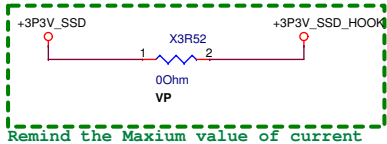
PEGATRON DT-MB RESTRICTED SECRET

<Variant Name>		Title : 038 - TP/CAM	
PEGATRON			
PEGATRON CORPORATION			
Size	Project Name	Rev	
A3	IPCML-CL	A00	
Date: Thursday, July 25, 2019		Sheet 38 of 97	



M.2 KEY-M for SSD (SATA+PCIE X4)

NOTE SCP#
(SSD crash portection for SSD dirty shutdown and BIOS shutdown.)
To prevent SSD corruption after ungraceful shutdown.
support NVMe: YES.
support SATA: NO.
support Optane :TBD.



+3P3VSB for MINI
I_{max}=2A /TDC=1.4A

+3P3V WLAN
RF solution.CAP close to Pin 2 &P72.

RF requirement

13 BT_PCMCLK_R
13 BT_PCMFRM_R
13 BT_PCMIN_R
13 BT_PCMOUT_R

X3R21 1
X3R22 1

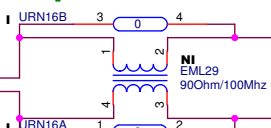
2 0 BT_PCMFRM_R_RSTN
2 0 BT_PCMOUT_R_CLKREQ0

6
8
10
12
14
16

LED1#
PCM_CLK
PCM_SYNC/LCP_RSTN
PCM_IN
PCM_OUT/CLKREQ0
LED2#

KEY-E

note:space issue can't change ECMF

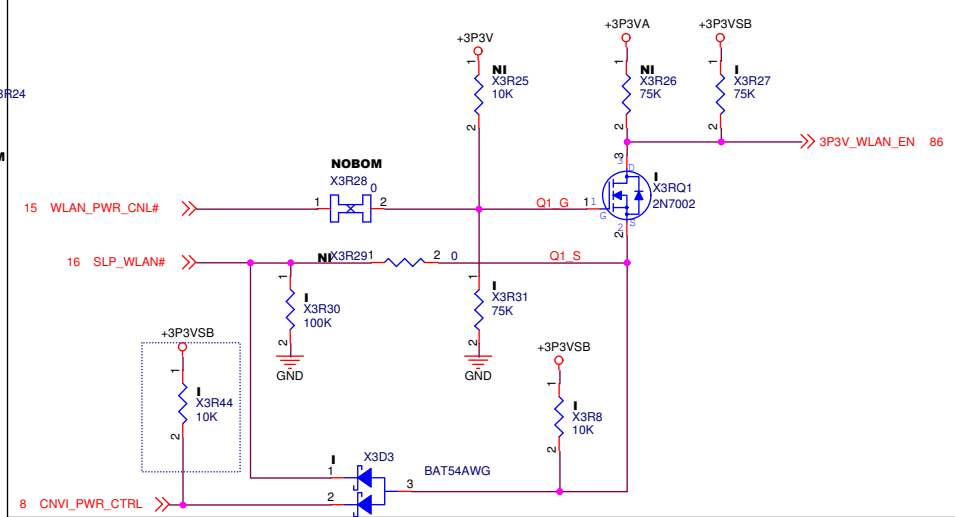


CNVi

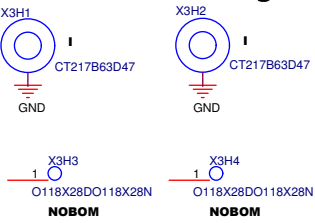
WLAN

CNVi

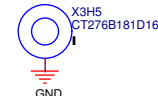
CNVi & PICE WLAN CARD POWER EN CIRCUIT



For WiFi shielding



for M2 conn H=3.1 mm

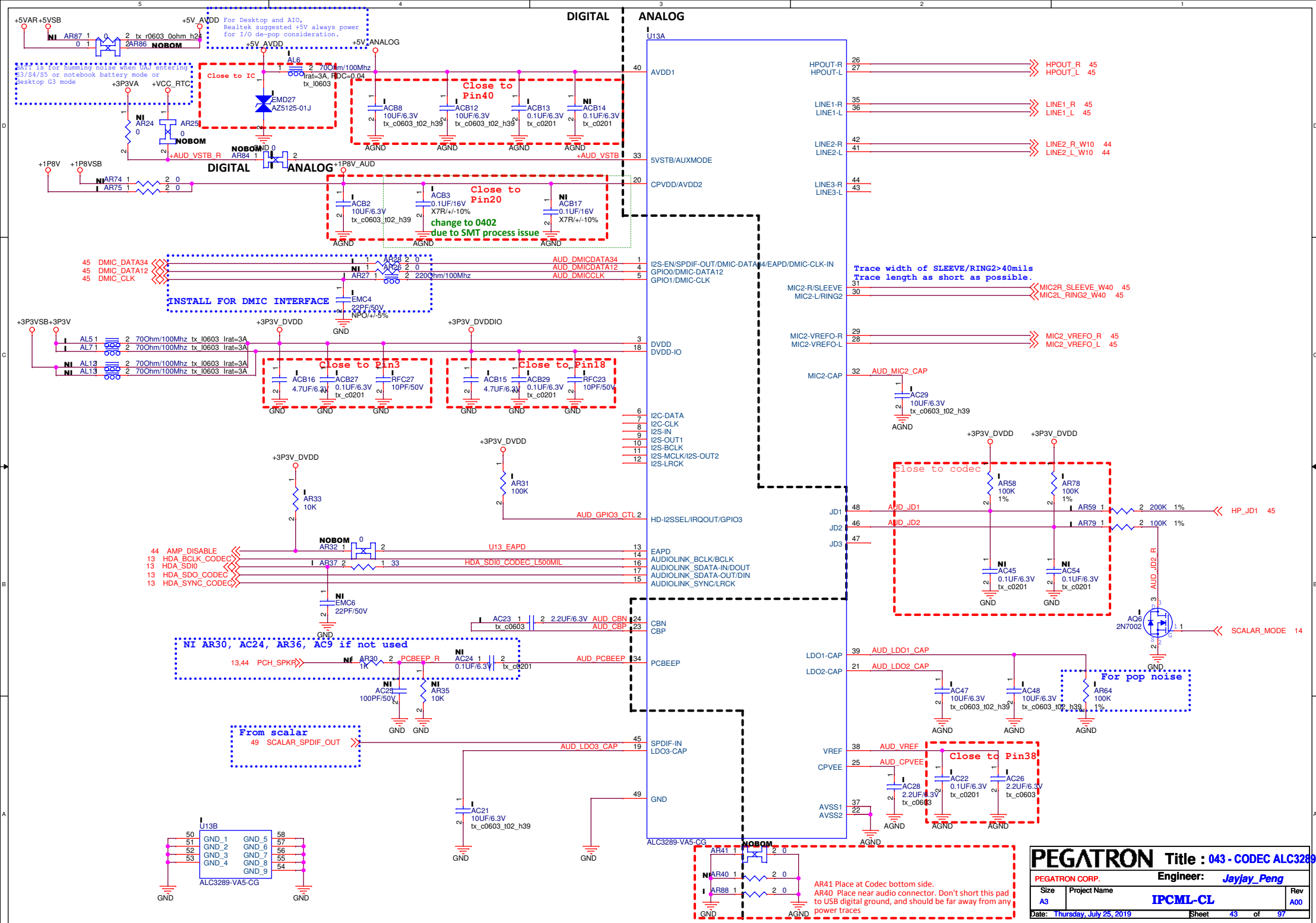


PEGATRON Title : 042-WLAN_M2 KEY E

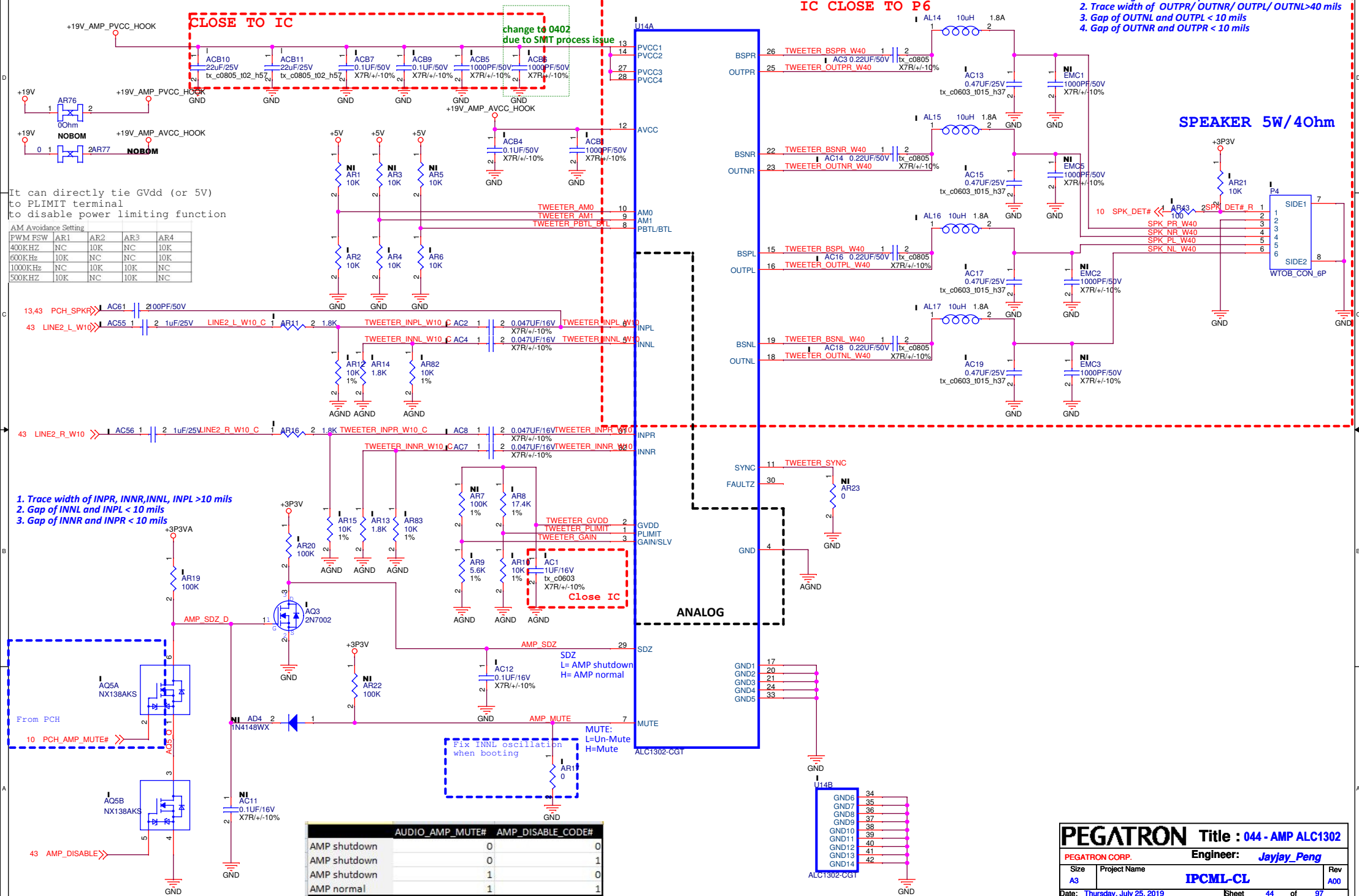
PEGATRON CORPORATION Engineer: Jayjay_Peng

Size A3 Project Name IPCML-CL Rev A00

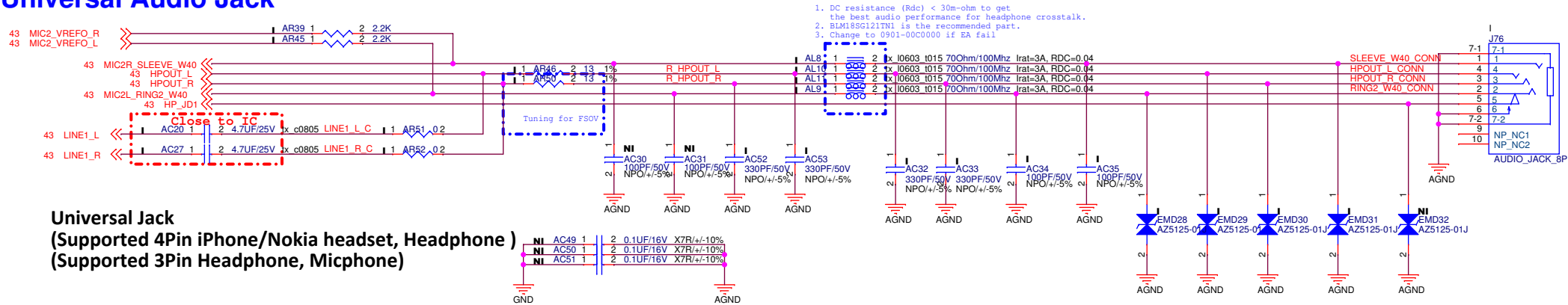
Date: Thursday, July 25, 2019 Sheet 42 of 97



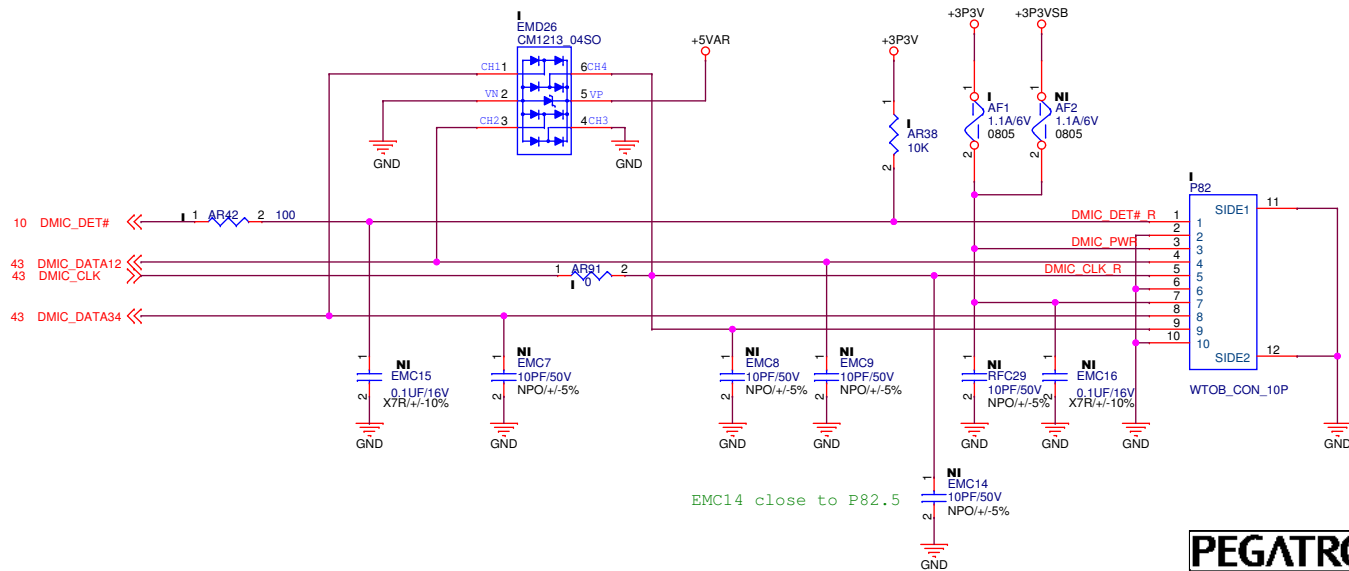
PVCC/AVCC SOURCE AND CAPS ARE SELECTED BY PROJECT
SPEC:MAX 30V, RECOMMEND 4.5~24V



Universal Audio Jack



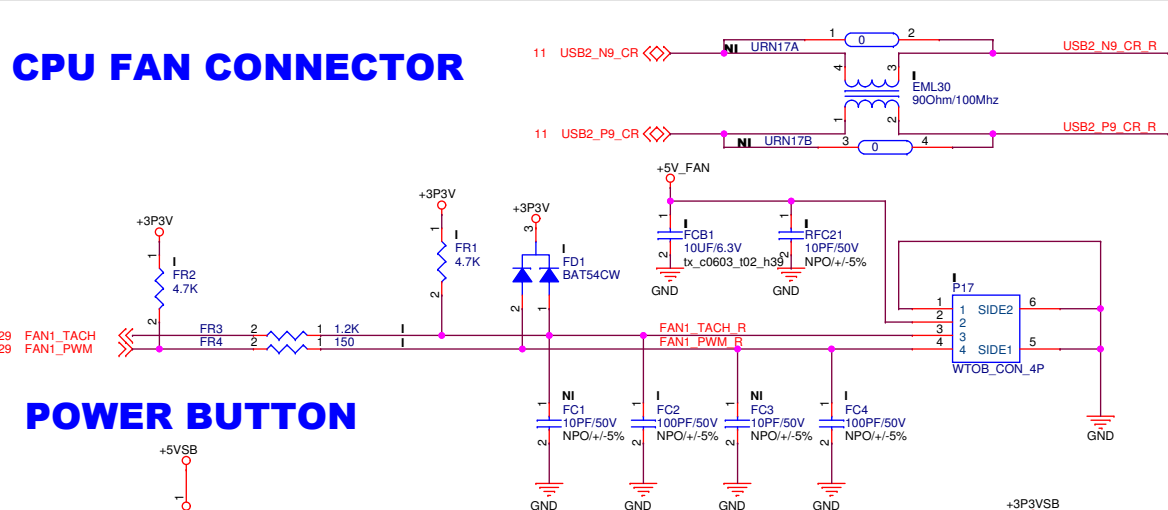
DMIC HEADER



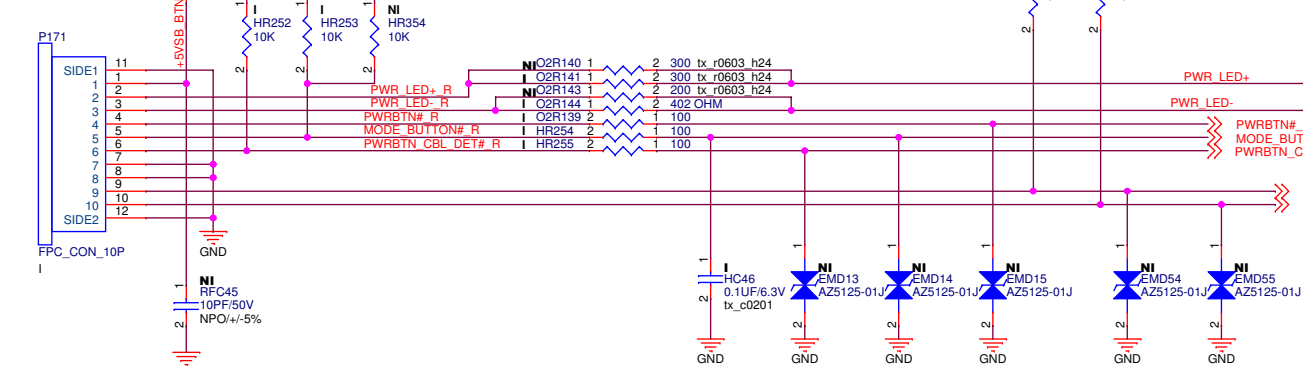
CPU FAN CONNECTOR

POWER BUTTON

SATA HDD CONNECTOR



FAN/CR: Follow Punisher-KBL



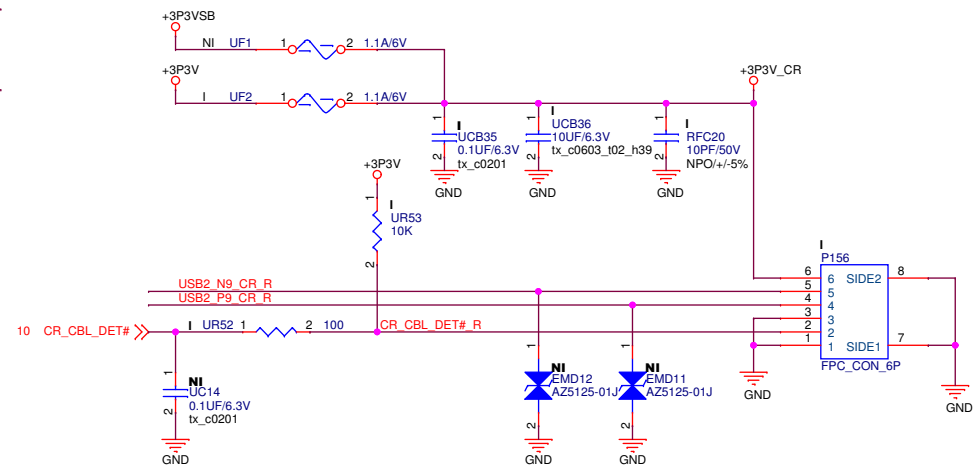
NOTE:

Place those Cap close to Conn sode
To Conn distance are less then 500mils

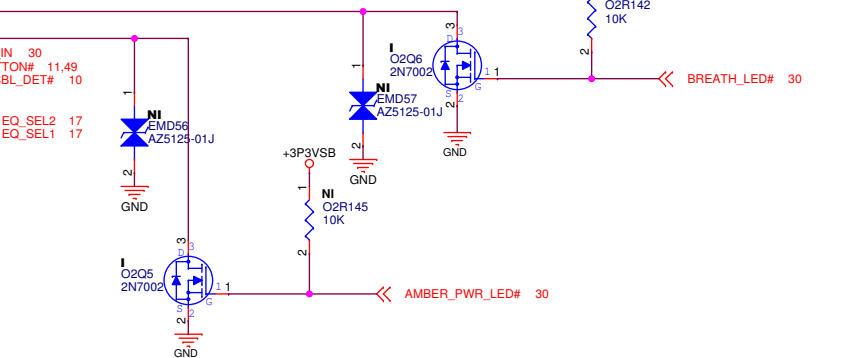
SATA: Follow Punisher-KBL

change to 0402
due to SMT process issue

Card reader CONNECTOR



EVERLIGHT
Amber Vf=1.7V~2.4V(PWR_LED+_R)
(5-1.7)^2/300=0.0363W (5-1.7)/300=0.011A
(5-2.4)^2/300=0.0225W (5-2.4)/300=0.0086A
White Vf=2.7V~3.7V(PWR_LED+_R)
(5-2.7)^2/200=0.0265W (5-2.7)/200=0.0115A
(5-3.7)^2/200=0.00845W (5-3.7)/200=0.0065A

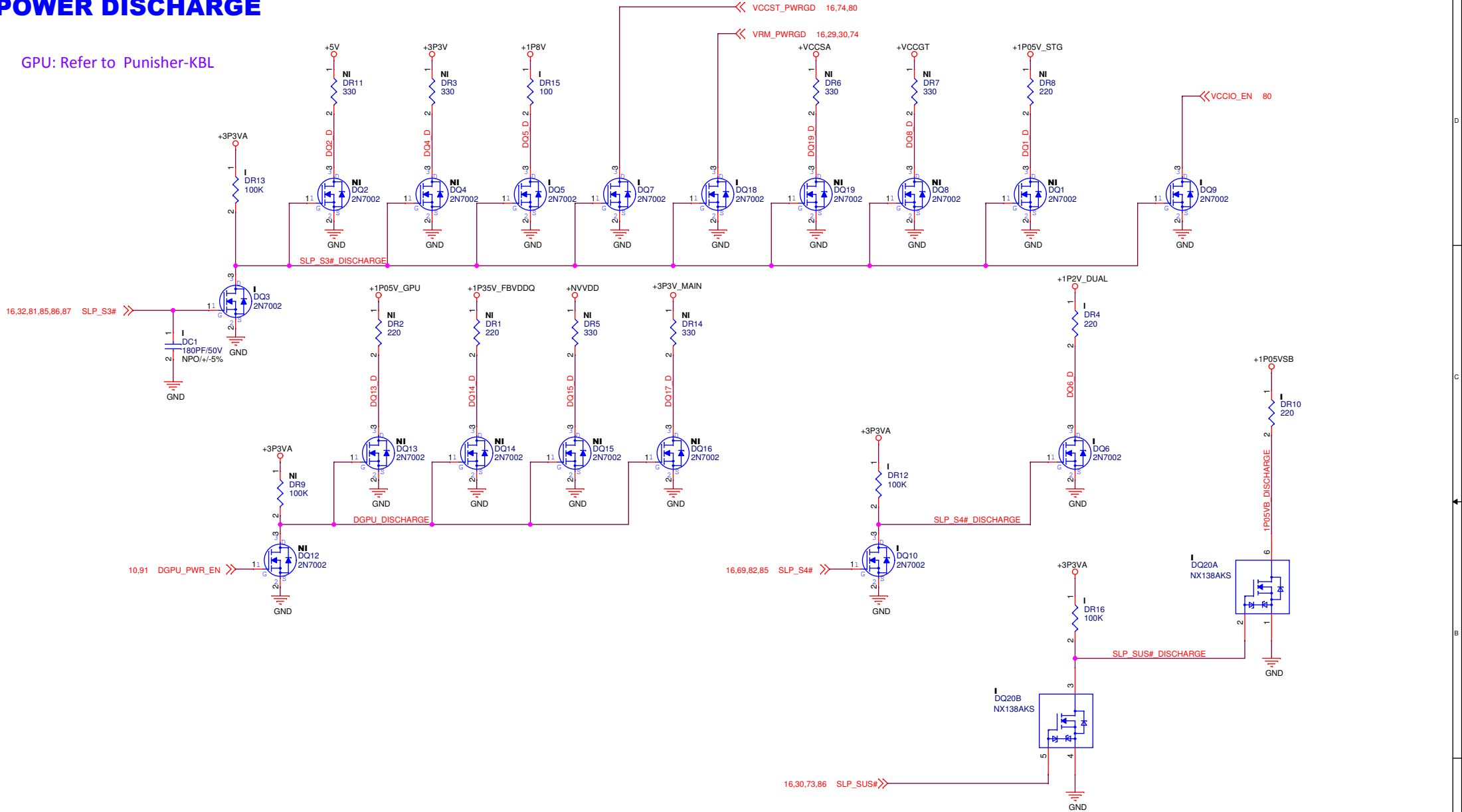


2018-1023 :Update

Breath_LED#	Amber_LED#	WHITE LED	AMBER LED
1	0	ON	OFF
0	1	OFF	ON
0	0	OFF	OFF

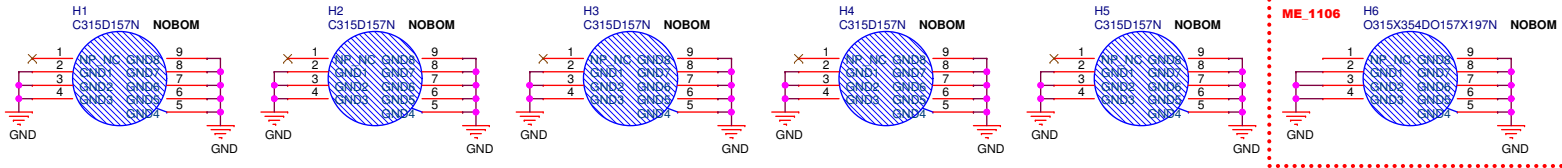
POWER DISCHARGE

GPU: Refer to Punisher-KBL



SCREW

MB PPID Need change to 15X100013000 (MX_LB1_LOGO_472X472)



CPU HOLE

GPU HOLE

PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title 947 - Discharge/SCREW

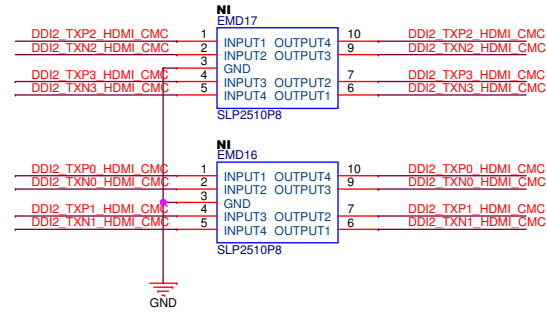
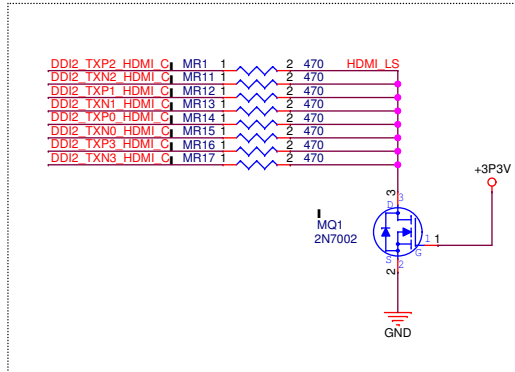
PEGATRON CORPORATION Engineer: Jayjay_Peng

Size	Project Name	Rev
A3	IPCM-L-CL	A00

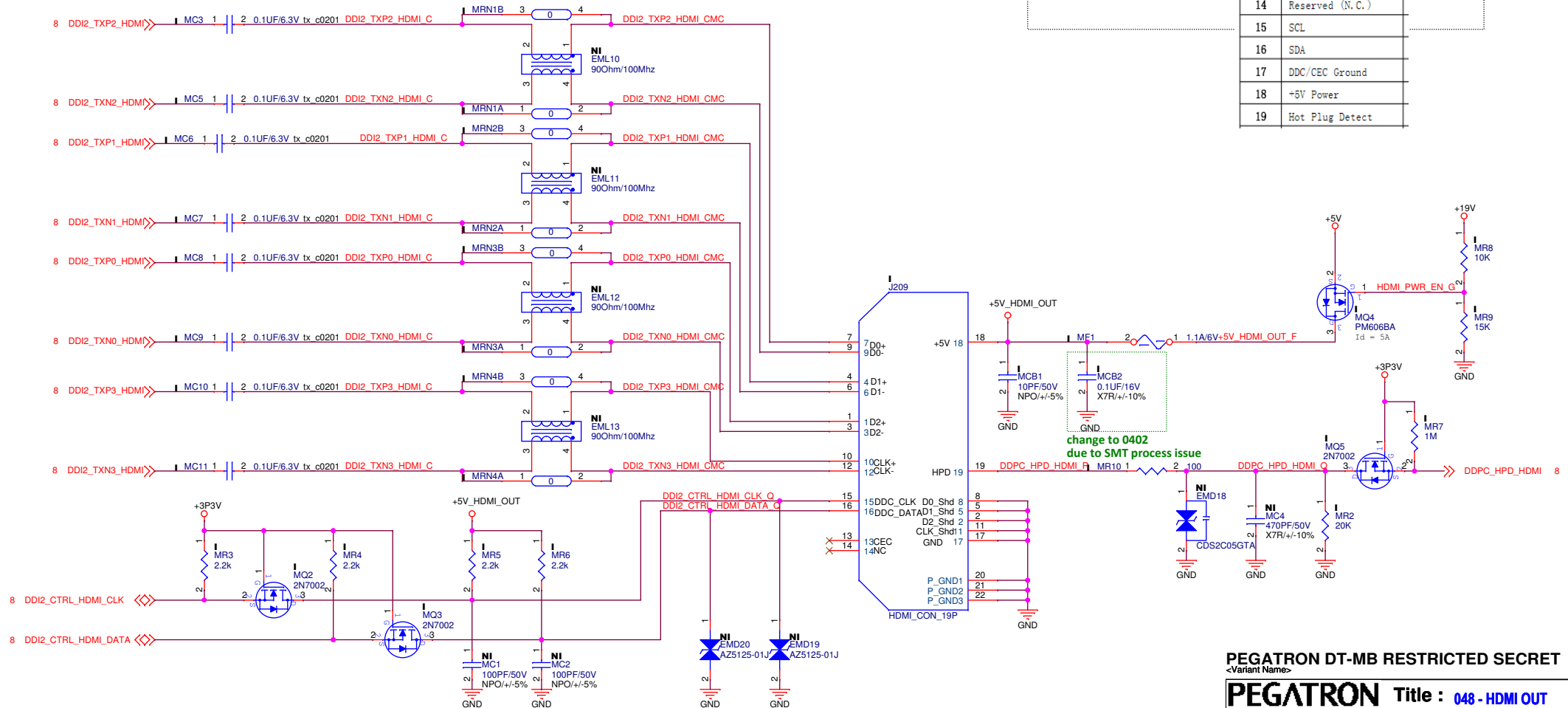
Date: Thursday, July 25, 2019 Sheet 47 of 97

HDMI: Follow Punisher-KBL

ESD Protection



1	TMDS Data2+
2	TMDS Data2 Shield
3	TMDS Data2-
4	TMDS Data1+
5	TMDS Data1 Shield
6	TMDS Data1-
7	TMDS Data0+
8	TMDS Data0 Shield
9	TMDS Data0-
10	TMDS Clock+
11	TMDS Clock Shield
12	TMDS Clock-
13	CEC
14	Reserved (N.C.)
15	SCL
16	SDA
17	DDC/CEC Ground
18	+5V Power
19	Hot Plug Detect

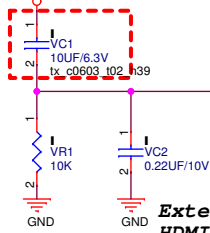


PEGATRON DT-MB RESTRICTED SECRET
~Variant Name~

PEGATRON Title : 048 - HDMI OUT
Engineer:

Size	Project Name	Rev
A3	IPCML-CL	A00
Date: Thursday, July 25, 2019	Sheet 48 of 97	

MSTAR CRB use 10uF/16V.
pega 10uF/16V only 0805 size.



External
HDMI Input

Internal
CPU HDMI

HDMI LEVEL SHIFT

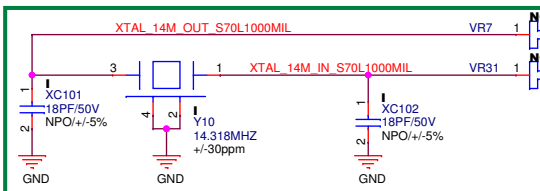


PCH UART for EDID update.
PCH SMBUS for FW update.

To codec

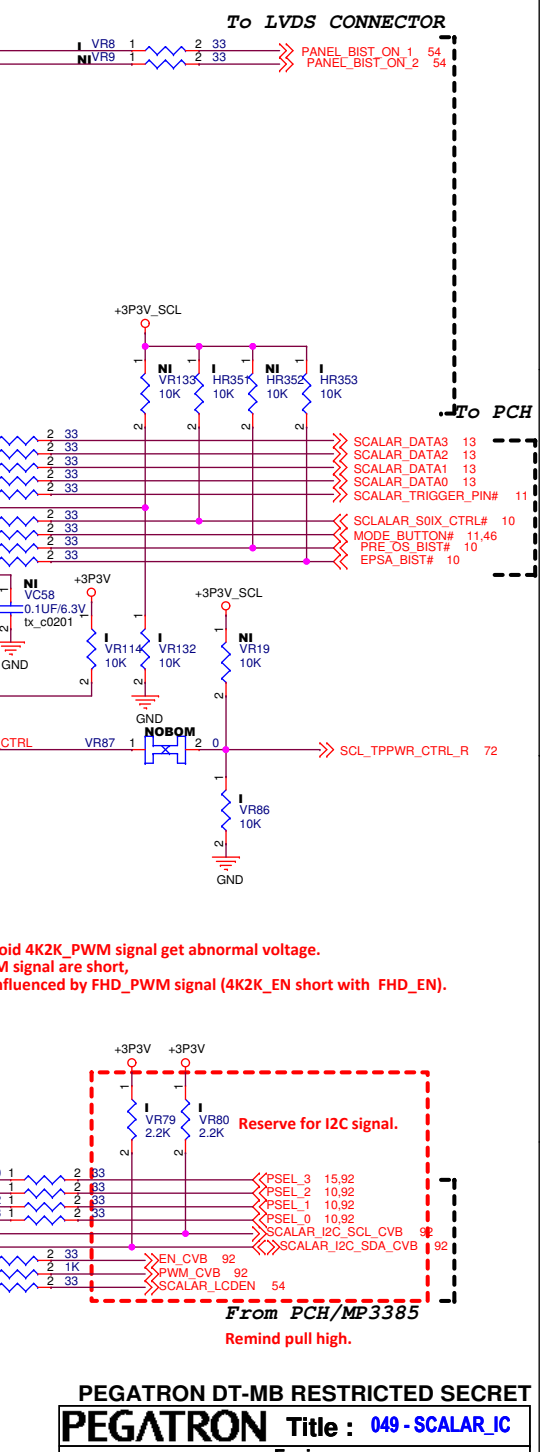
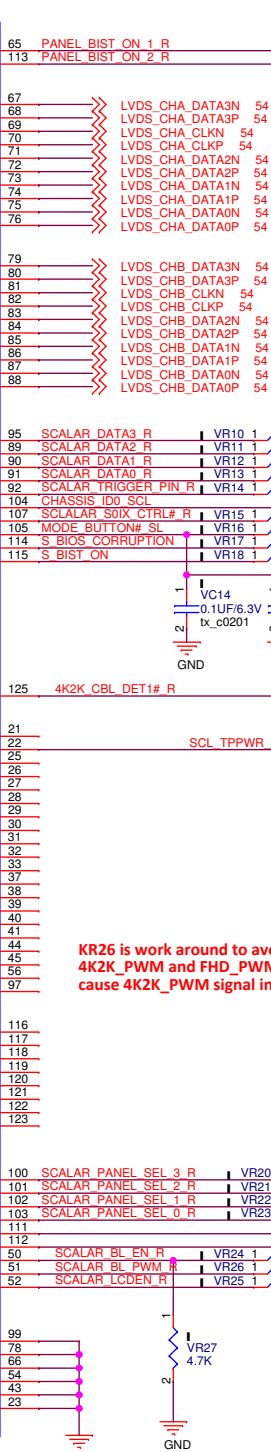
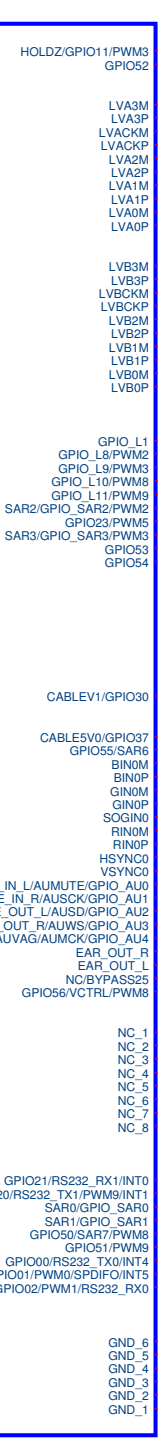
To EEPROM(HDCP KEY)

To SPI ROM(Scalar FW)

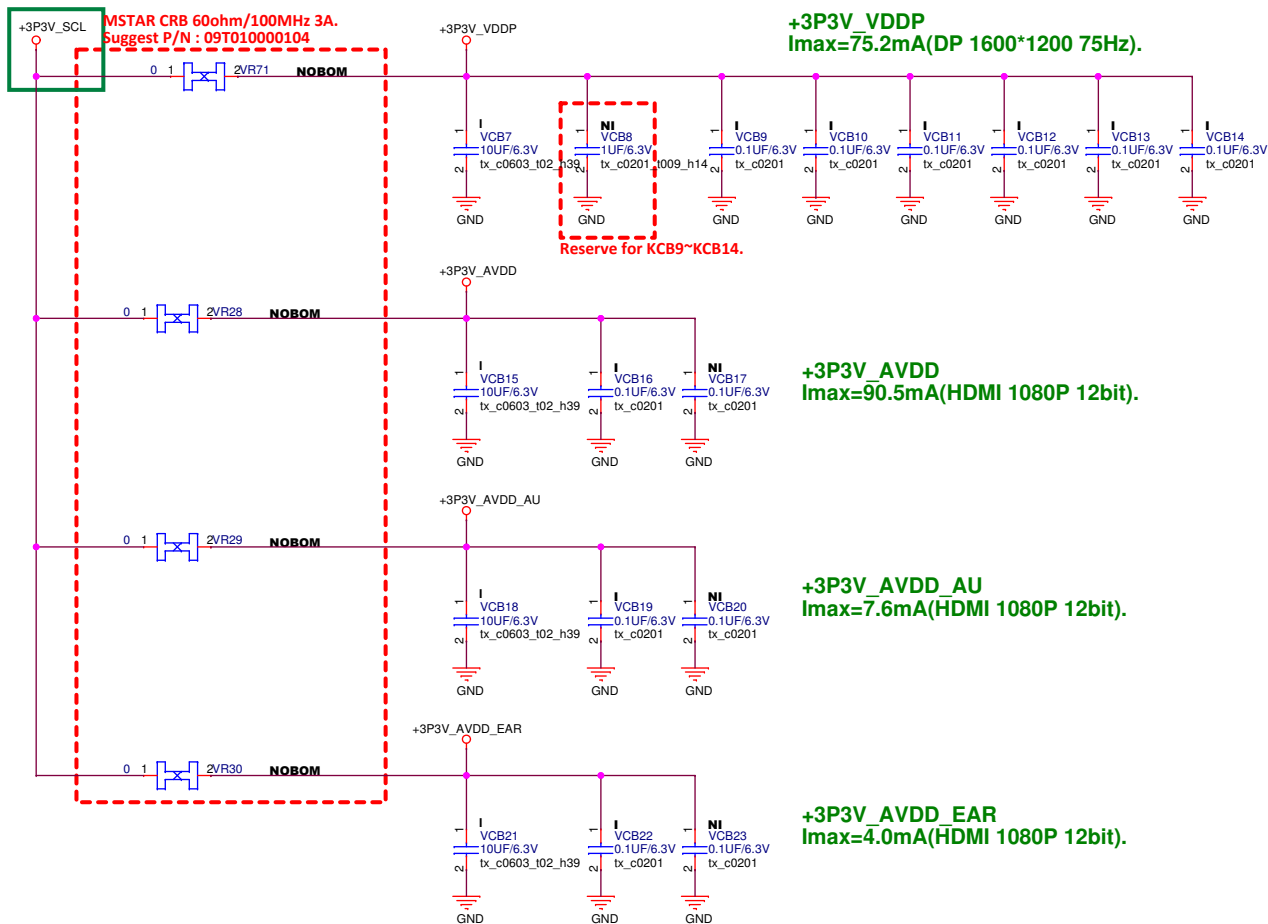


NOBOM VT1
NOBOM VT2
NOBOM VT3

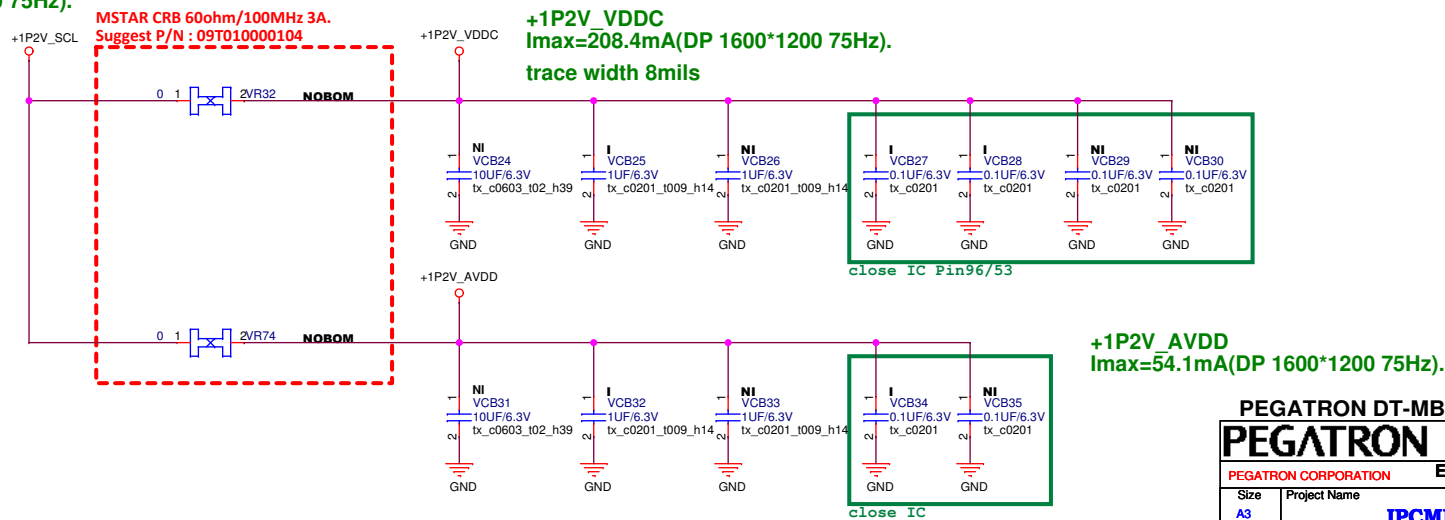
SCALAR TP1
SCALAR TP2
SCALAR TP3



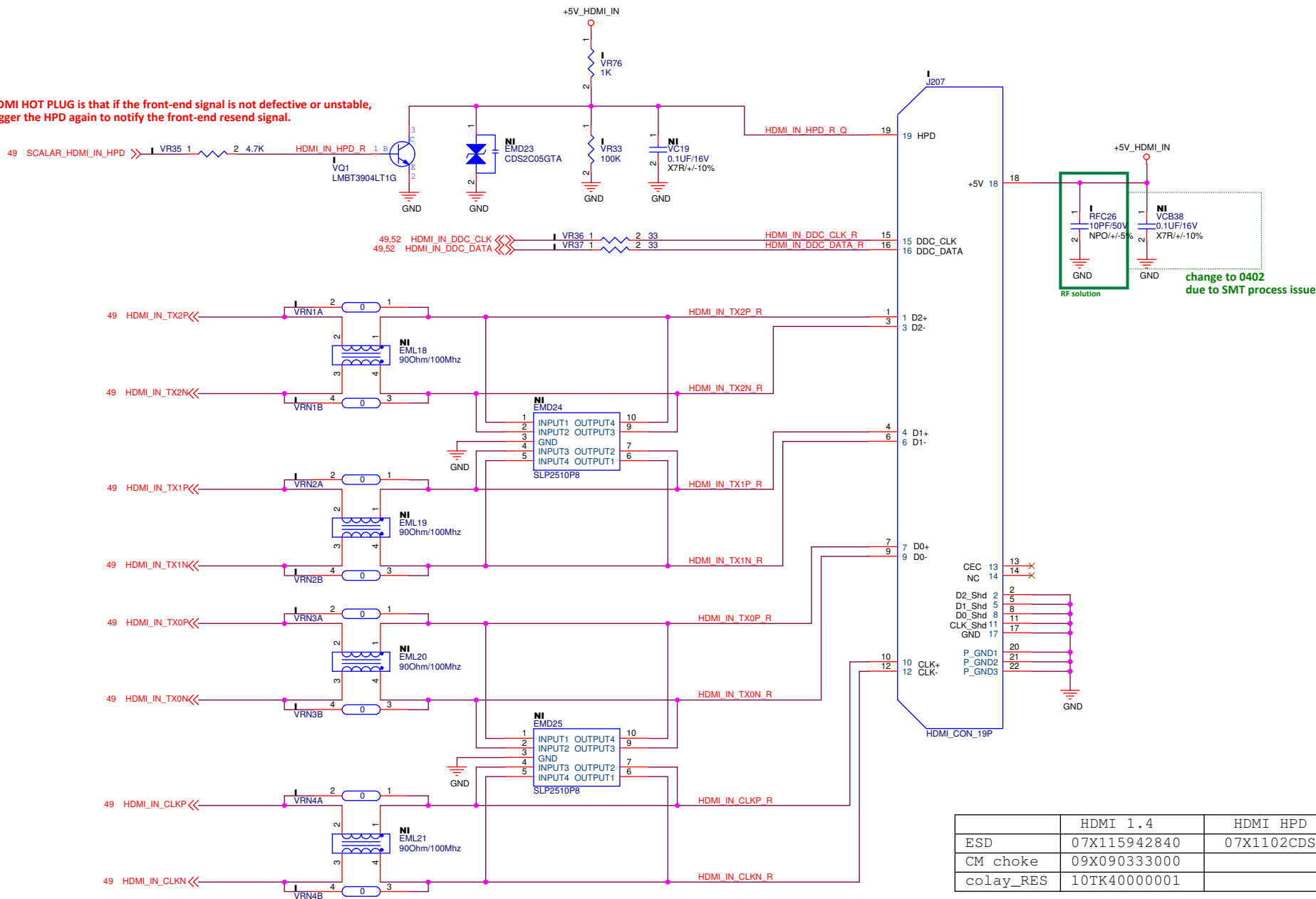
+3P3V
 $I_{max}=164.1mA(DP\ 1600*1200\ 75Hz).$
 trace width 8mils



+1P2V
 $I_{max}=262.4mA(DP\ 1600*1200\ 75Hz).$
 trace width 10mils

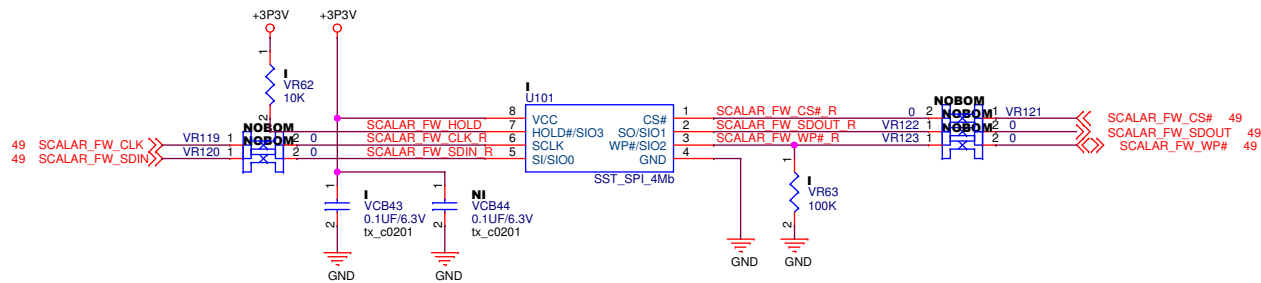


The role of HDMI HOT PLUG is that if the front-end signal is not defective or unstable, the IC can trigger the HPD again to notify the front-end resend signal.

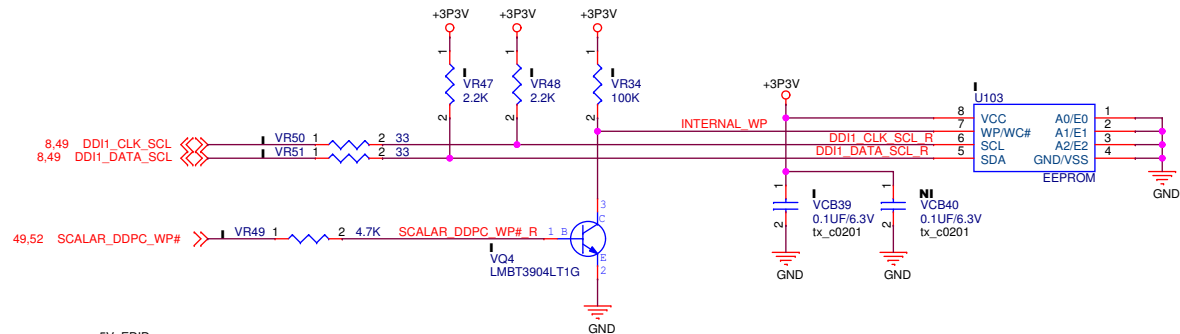


	HDMI 1.4	HDMI HPD
ESD	07X115942840	07X1102CDS20
CM choke	09X090333000	
colay_RES	10TK40000001	

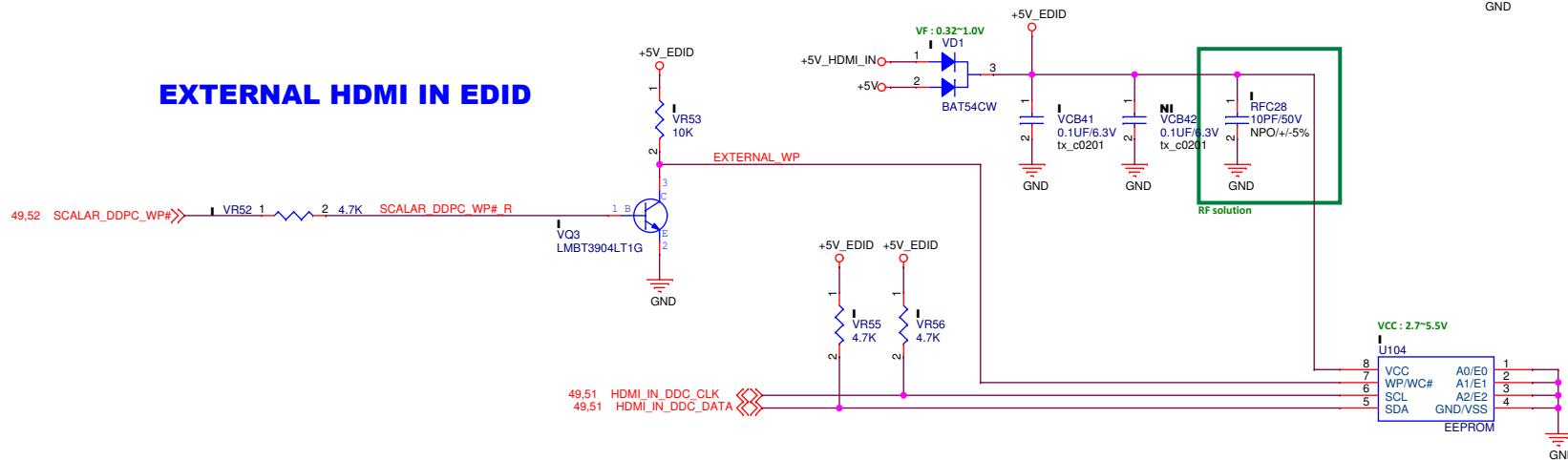
SCALAR SPI ROM



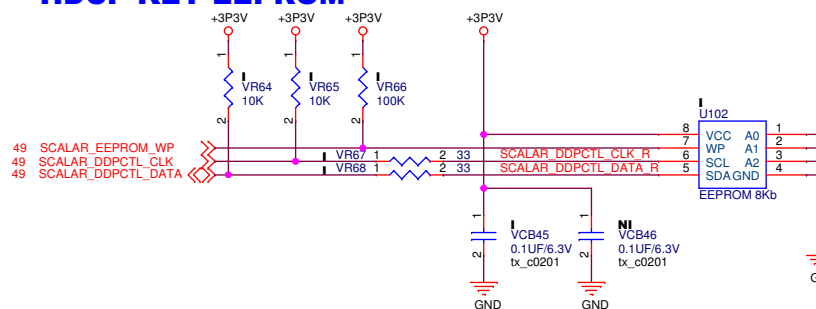
INTERNAL DISPLAY EDID



EXTERNAL HDMI IN EDID



HDPC KEY EEPROM



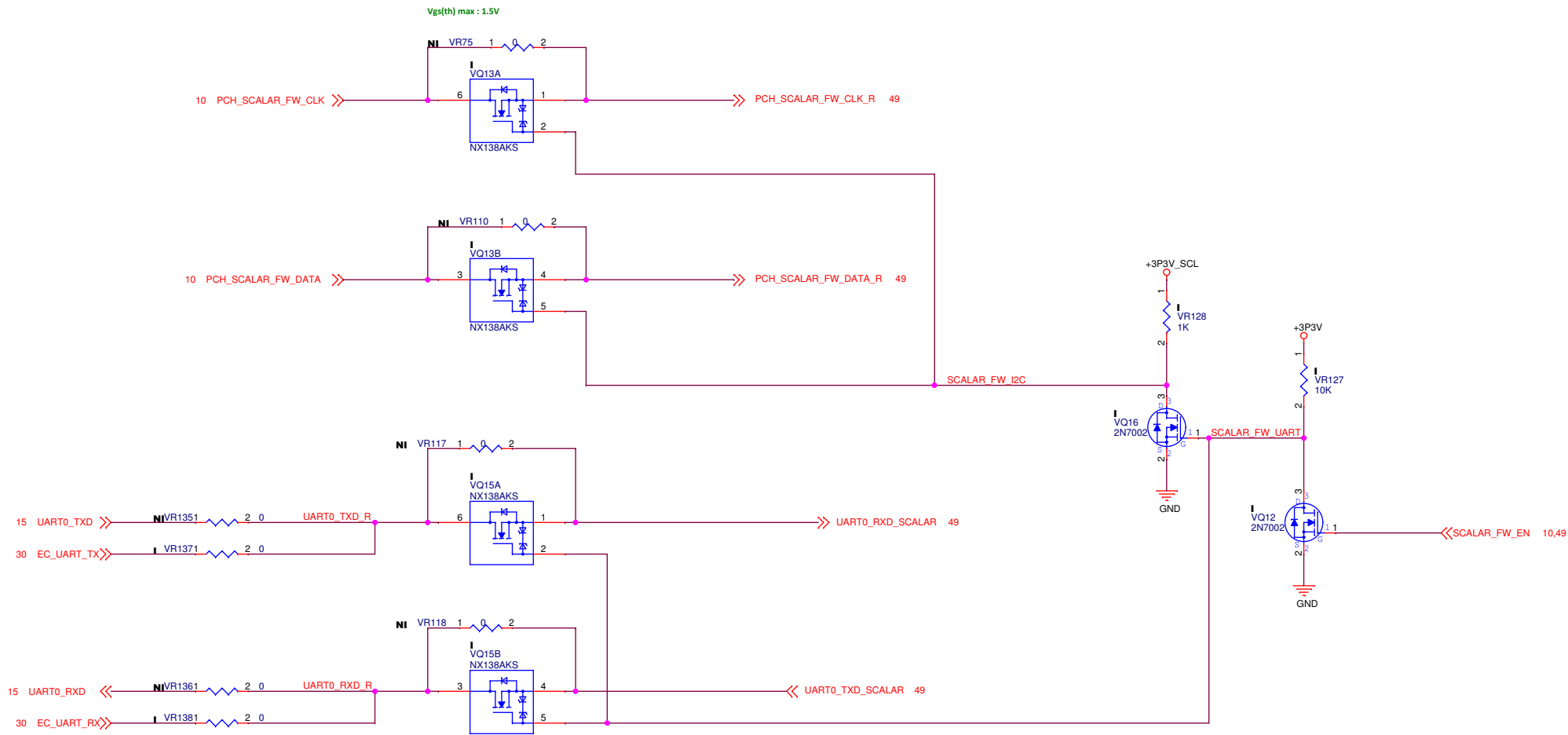
PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title : 052 - SCALAR_MISC 1.2

PEGATRON CORPORATION Engineer: **Bacan Hsu**

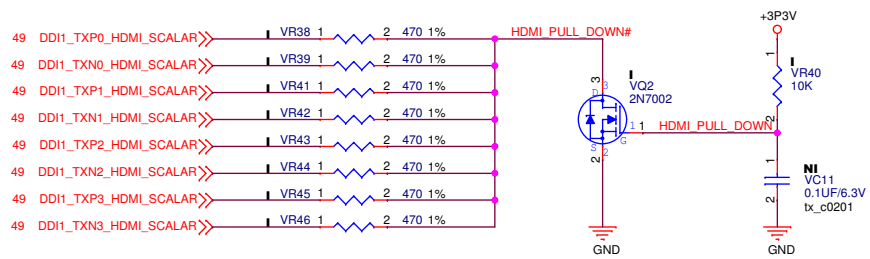
Size A3 Project Name **IPCML-CL** Rev A00

Date: Thursday, July 25, 2019 Sheet 52 of 97

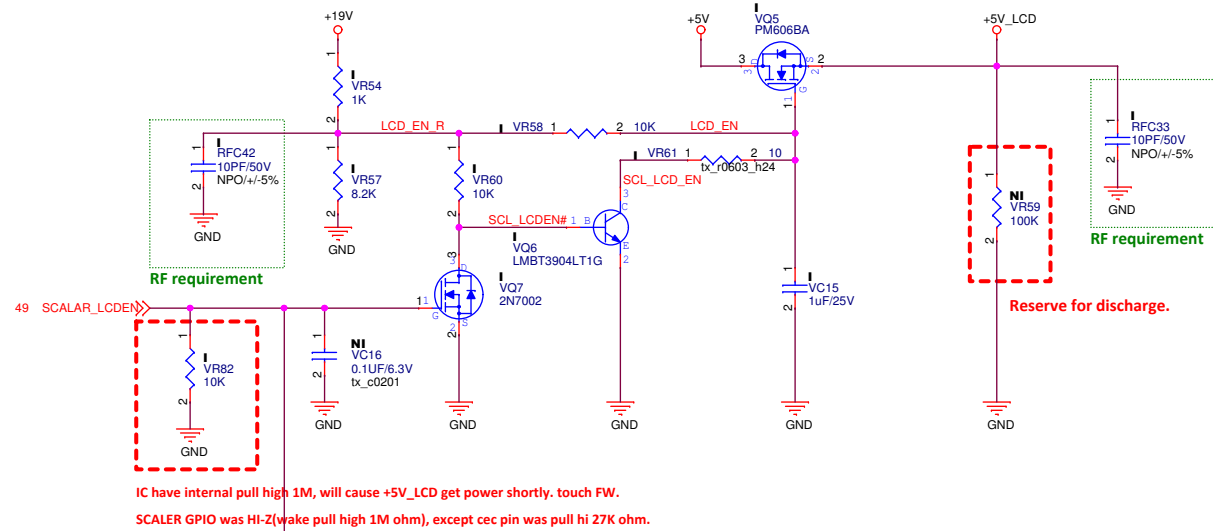


SCALAR HDMI LEVEL SHIFT (Cost Reduce)

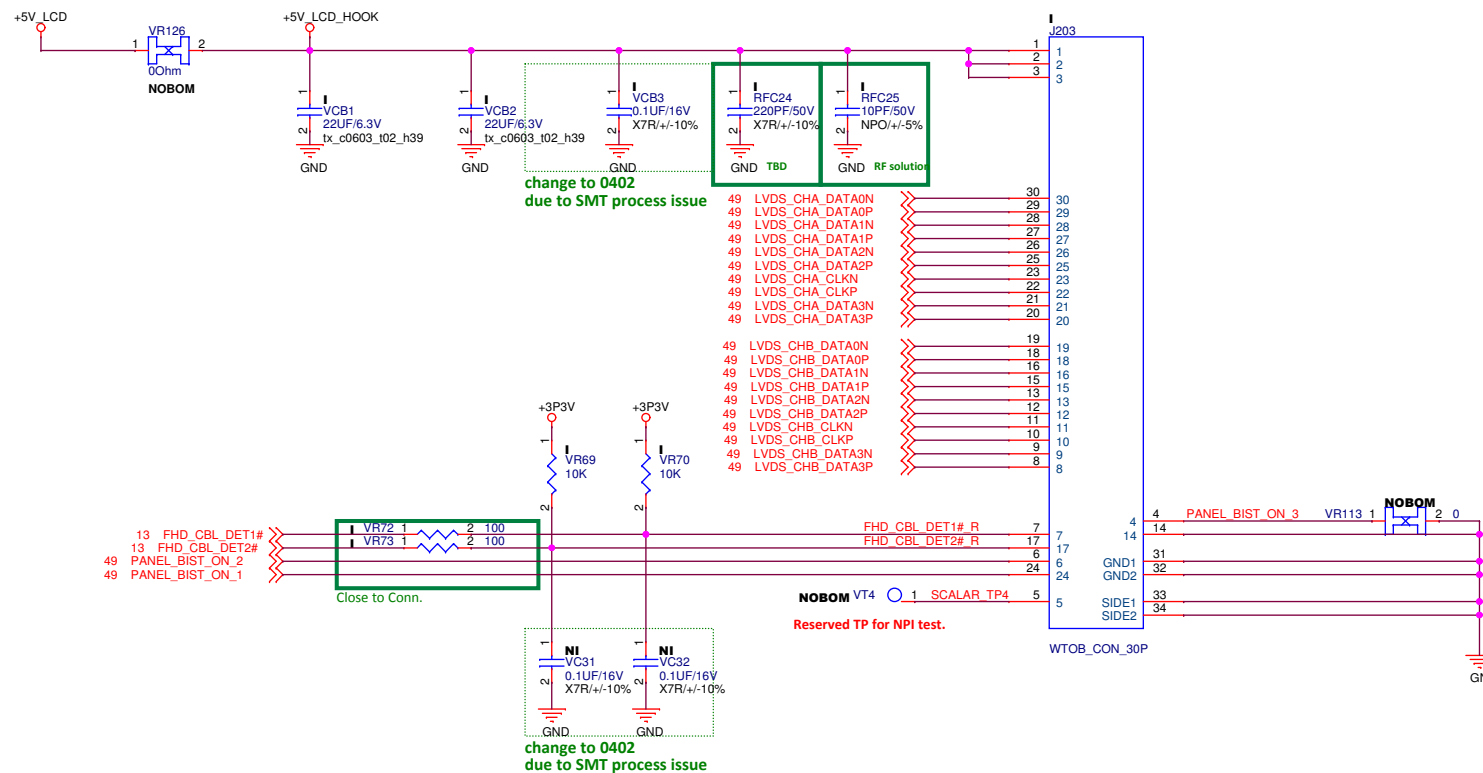
Cost Reduced Level Shifter Motherboard Topology for max data rate of 1.65 Gb/s
Active Level Shifter Motherboard Topology for max data rate of 2.97 Gb/s

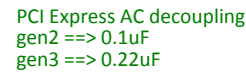


PANEL POWER Controller



FHD Connector

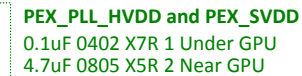




+1P05V_GPU



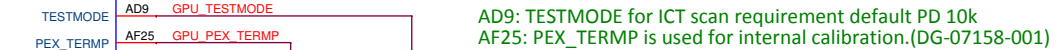
+3P3V_AON



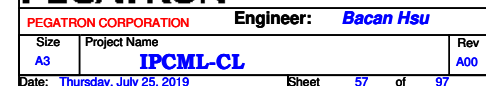
0.1uF 0402 X7R 1 Under GPU
1uF 0603 X5R 1 Near GPU
4.7uF 0805 X5R 1 Near GPU



+PEX

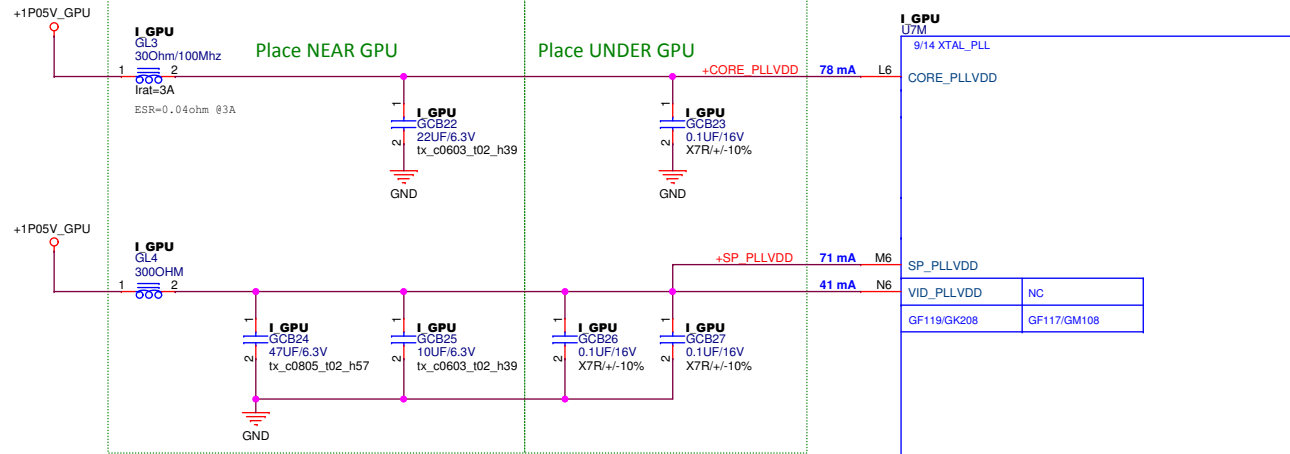


PEGATRON CORPORATION		Engineer:	Bacan Hsu
Size A3	Project Name IPCML-CL		Rev A00
Date: Thursday, July 25, 2019		Sheet	56 of 97



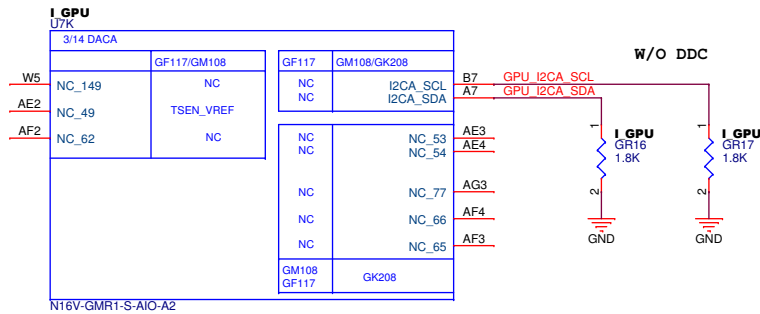
CORE_PLLVDD

0.1uF 0402 X7R 1 Under GPU
22uF 0805 X5R 2 Near GPU

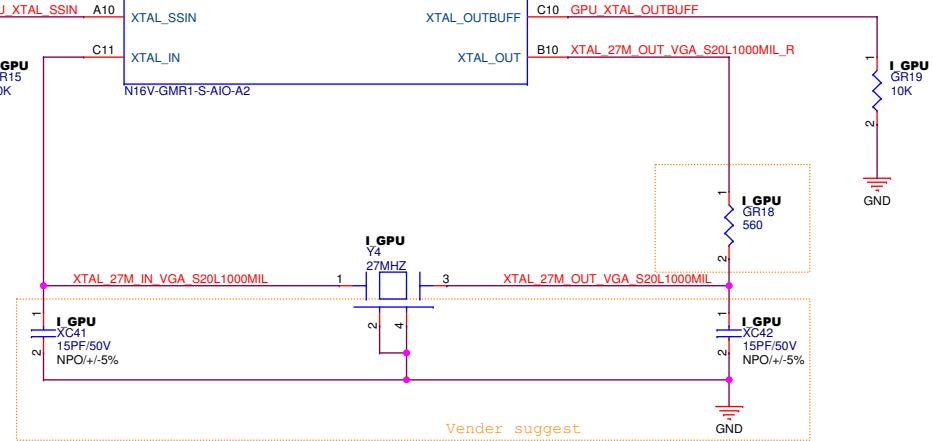


SP_PLLVDD + VID_PLLVDD

0.1uF 0402 X7R 2 Under GPU
10uF 0603 X5R 1 Near GPU
47uF 0805 X5R 1 Near GPU



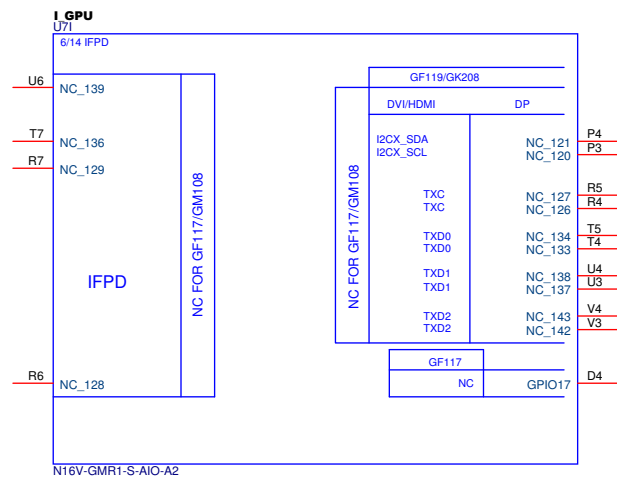
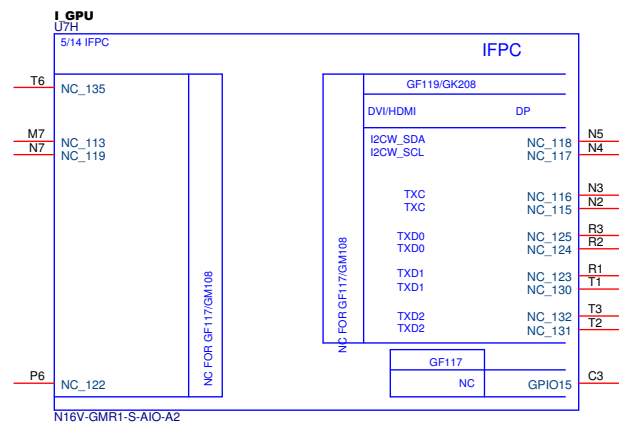
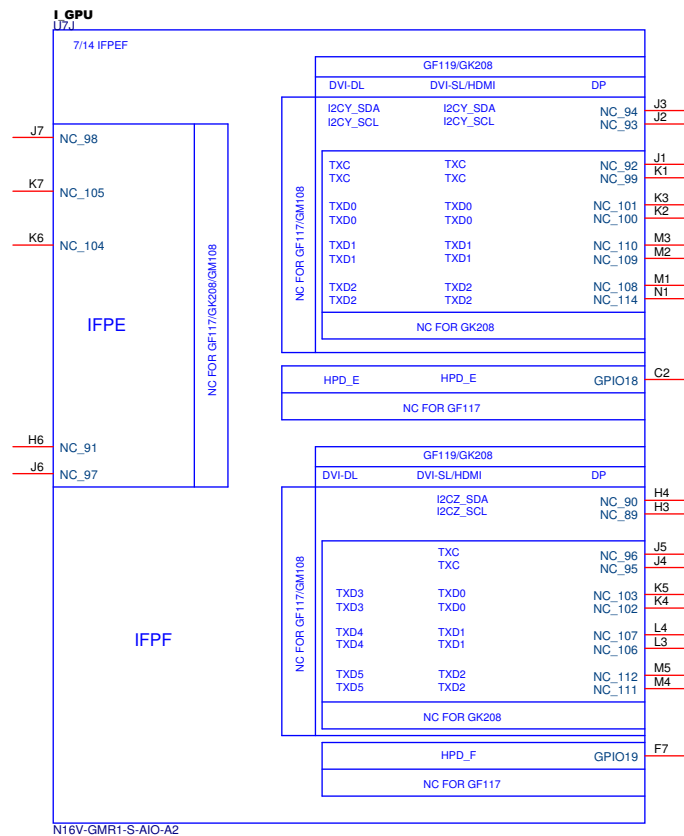
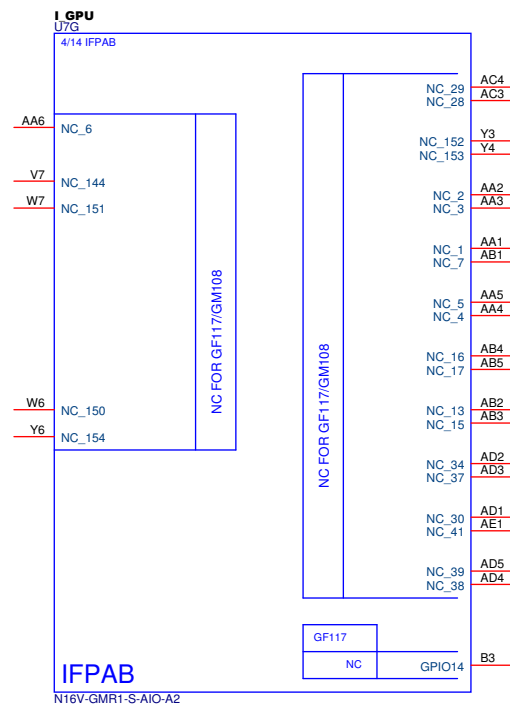
STUFF PDs on XTALSSIN and XTALOUTBUFF WHEN EXT_SS IS NOT USED



PEGATRON DT-MB RESTRICTED SECRET
<Variant Name>

PEGATRON		Title : 038 - N16V-GMR1_DAC_A_XTAL	
PEGATRON CORPORATION		Engineer: Bacan Hsu	
Size A3	Project Name	Rev A00	
Date: Thursday, July 25, 2019		Sheet 58 of 97	

Display from CPU DDI,dGPU NC



PEGATRON DT-MB RESTRICTED SECRET

<Variant Name>

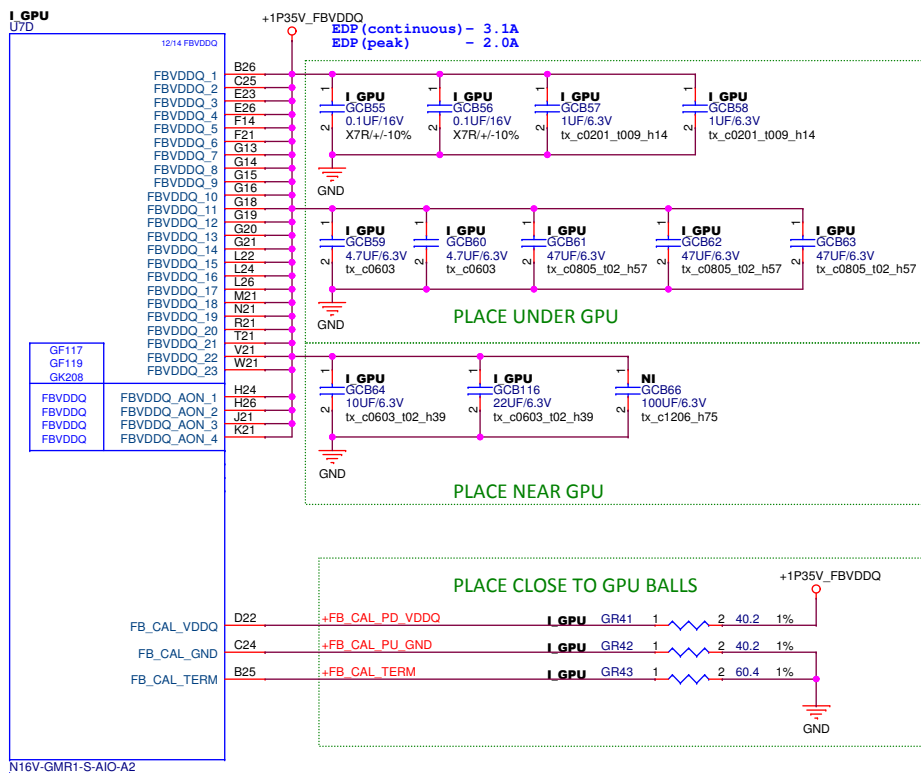
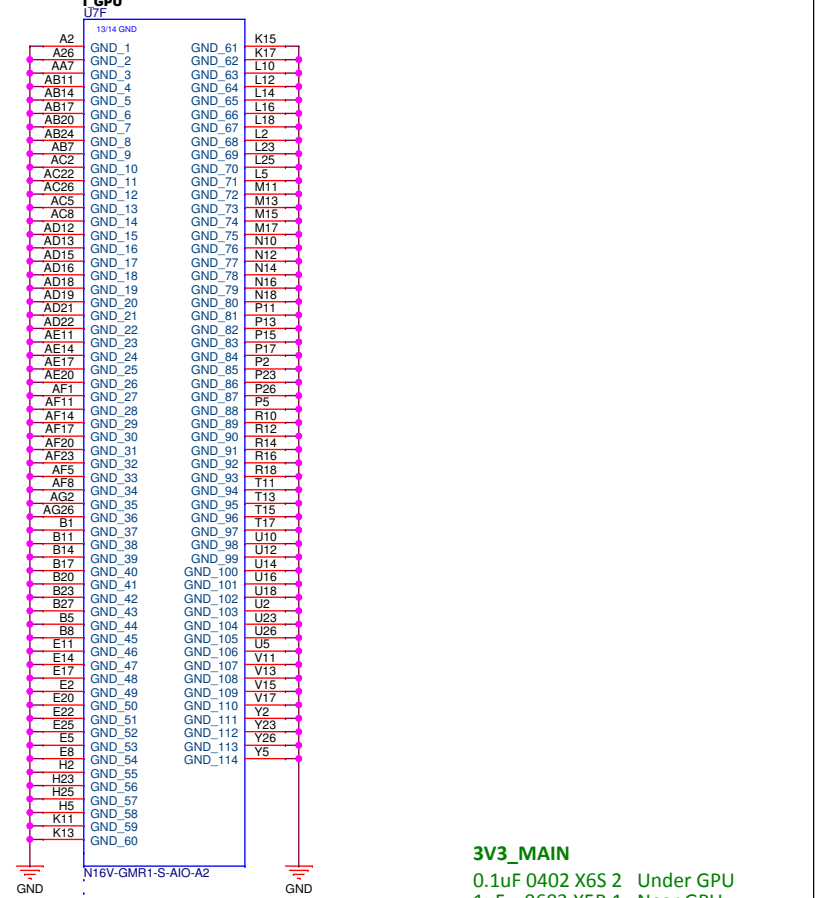
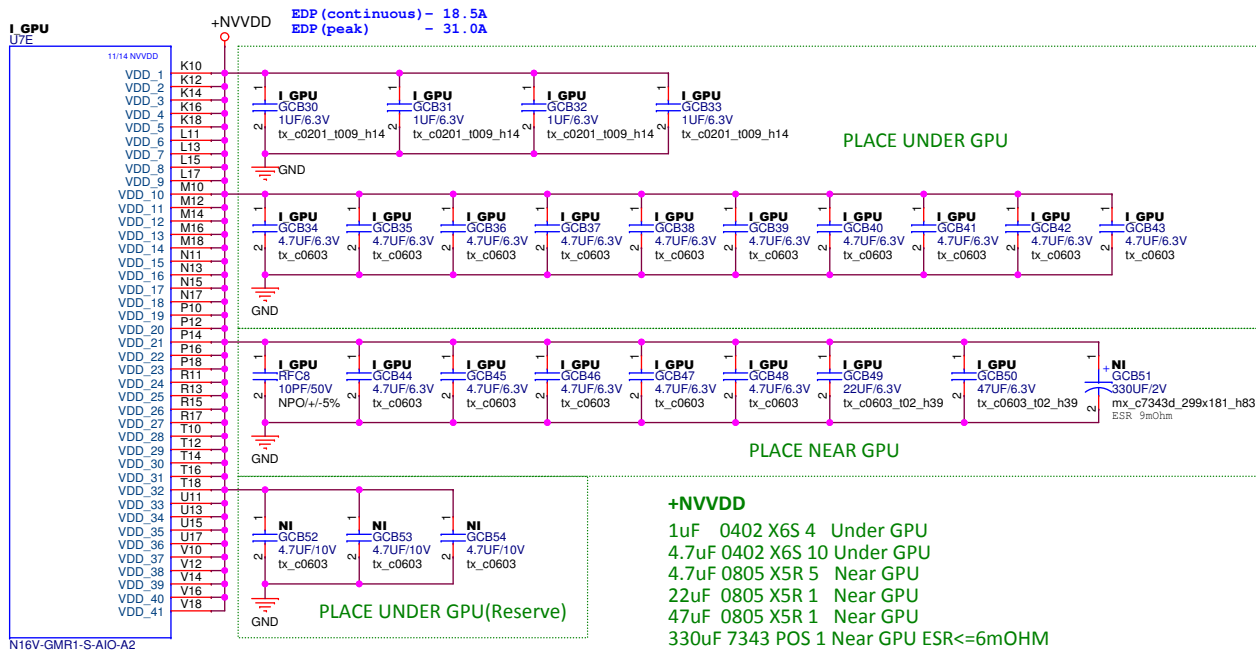
PEGATRON Title : 059 - N16V-GMR1_IFP_NC

PEGATRON CORPORATION Engineer: Bacan Hsu

Size Project Name Rev

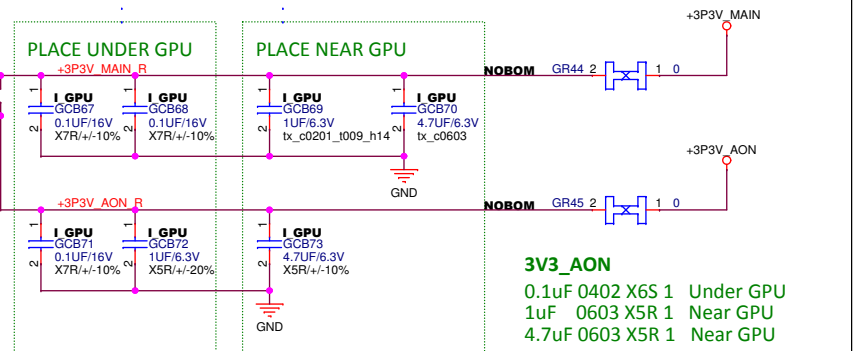
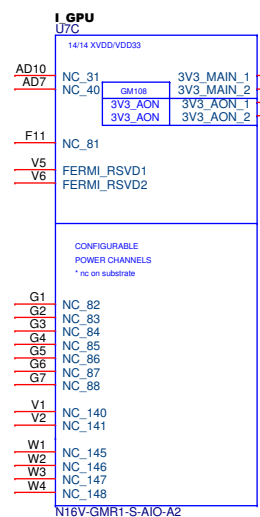
A3 IPCML-CL A00

Date: Thursday, July 25, 2019 Sheet 59 of 97



+FBVDDQ and +FBVDDQ

0.1uF 0402 X7R 2 Under GPU
1uF 0603 X7R 2 Under GPU
4.7uF 0603 X6S 2 Under GPU
10uF 0805 X5R 1 Near GPU
22uF 0805 X5R 1 Near GPU



Strap:ROM_SI for VRAM select 256Mx32 (D5U1+D5U2) = 2GB

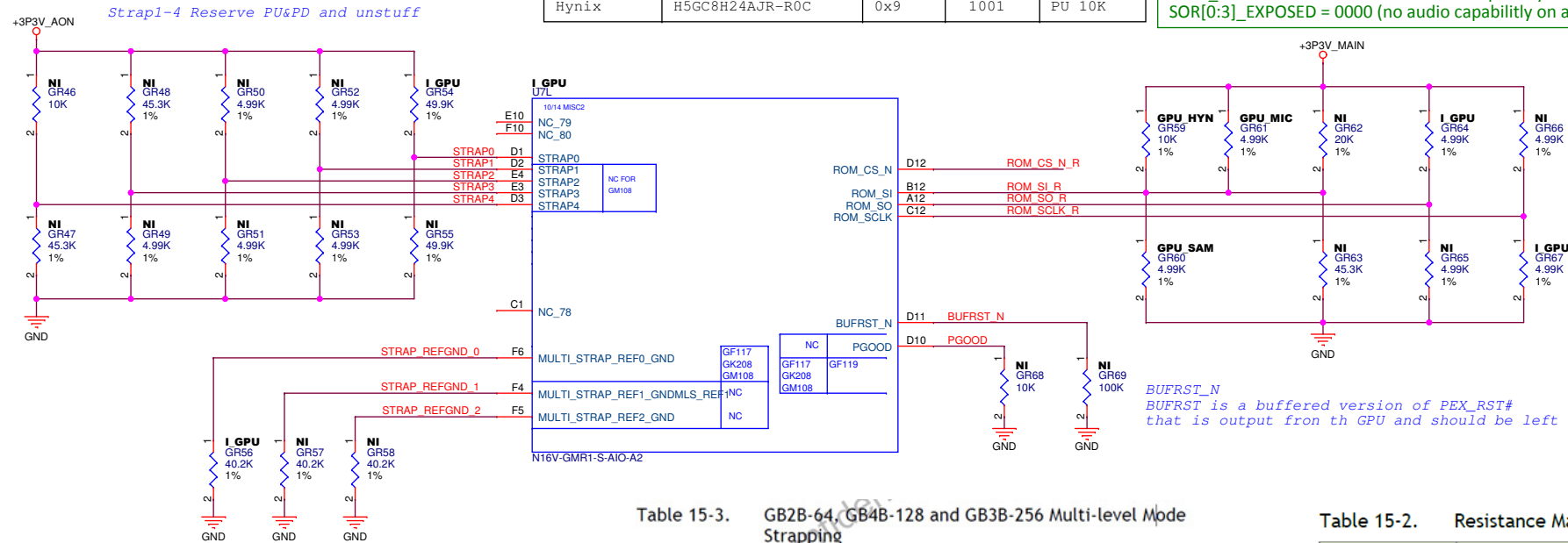
Vendor	Manufacturer P/N	Strap	Hex	
Samsung	K4G80325FB-HC28	0x0	0000	PD 4.99K
Micron	MT51J256M32HF-70:B	0x8	1000	PU 4.99K
Hynix	H5GC8H24AJR-R0C	0x9	1001	PU 10K

Strap:ROM_SO (1000 PU 4.99k)

DEVID_SEL=1 (Marketing name = MX110)
 PCIE_CFG=0 (Default)
 SMB_ALT_ADDR=0 (Default:0x9E)
 VGA_DEVICE=0 (MS Hybrid)

Strap:ROM_CLK (0000 PD 4.99k)

SORx_EXPOSED is used to define audio capability on each digital display
 SOR[0:3]_EXPOSED = 0000 (no audio capability on all digital display)



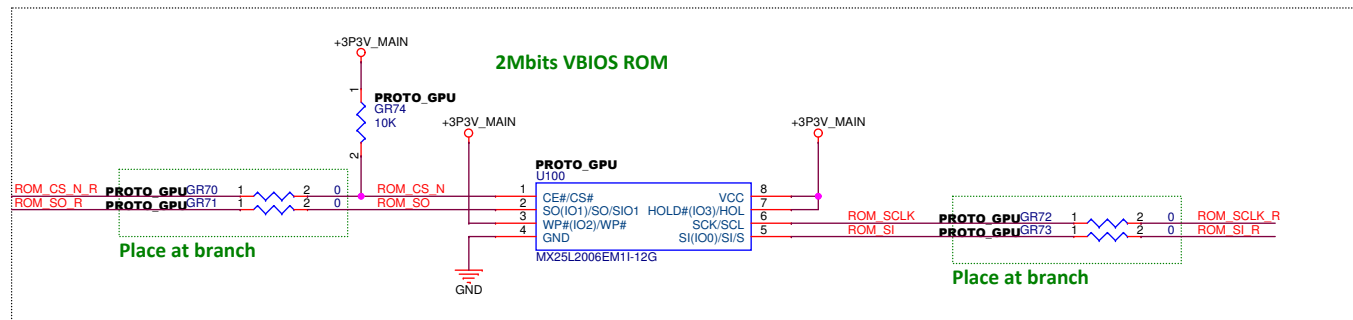
Multi_Strap_Ref0_GND
 To select different Strap mode,
 need to be stuffed accordingly(Default PD 40.2k 1%)

Table 15-3. GB2B-64, GB4B-128 and GB3B-256 Multi-level Mode Strapping

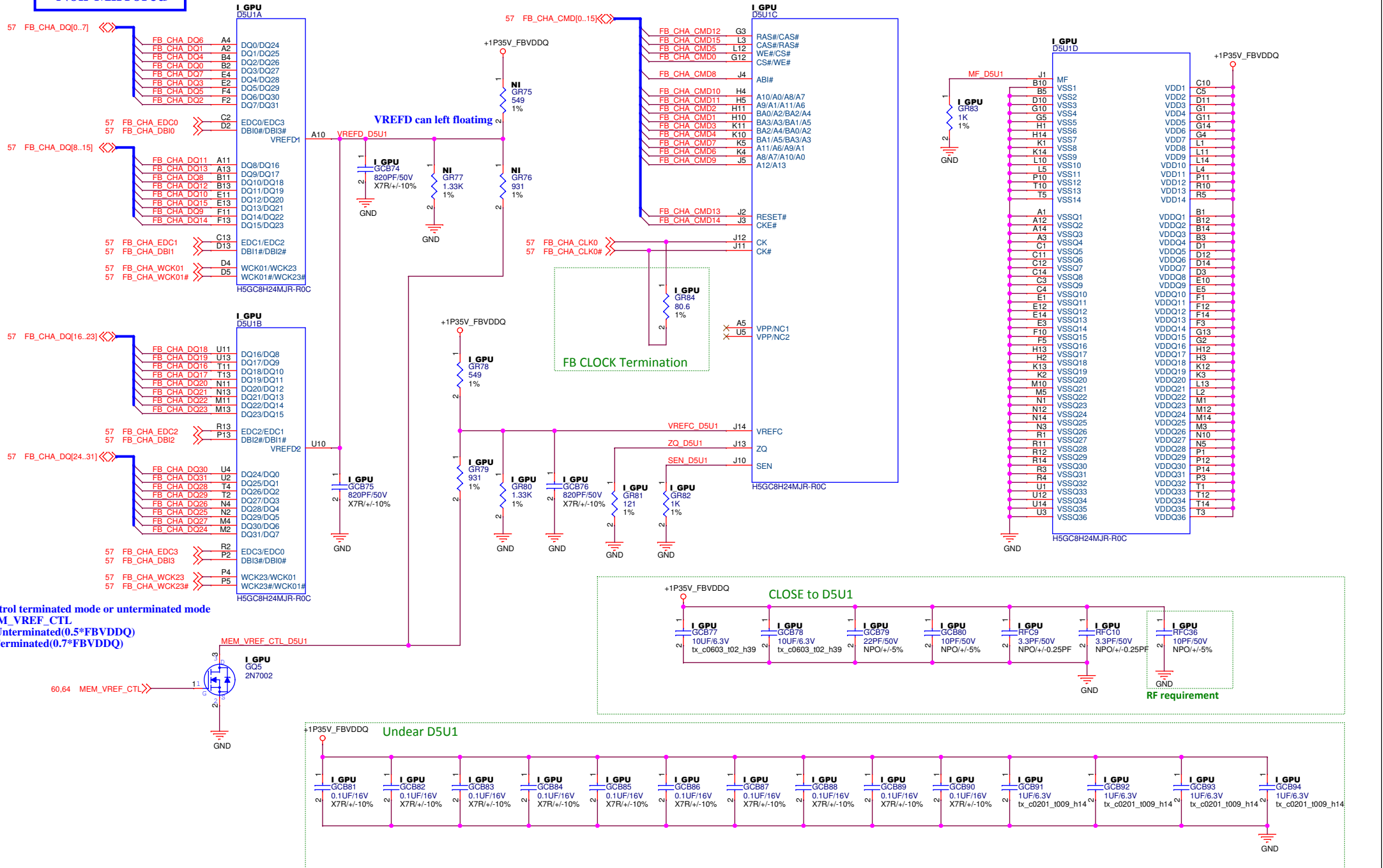
Strap Pin Name	Logical Strapping Bit 3	Logical Strapping Bit 2	Logical Strapping Bit 1	Logical Strapping Bit 0
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SI	RAM_CFG[3]	RAM_CFG[2]	RAM_CFG[1]	RAM_CFG[0]
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE
STRAP0	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Stuff 49.9 kΩ pull-up.			
STRAP1	Keep foot print for pull-up to 3V3_AON and pull-down to GND. Do not stuff.			
STRAP2				
STRAP3				
STRAP4				

Table 15-2. Resistance Mapping to Hex Values

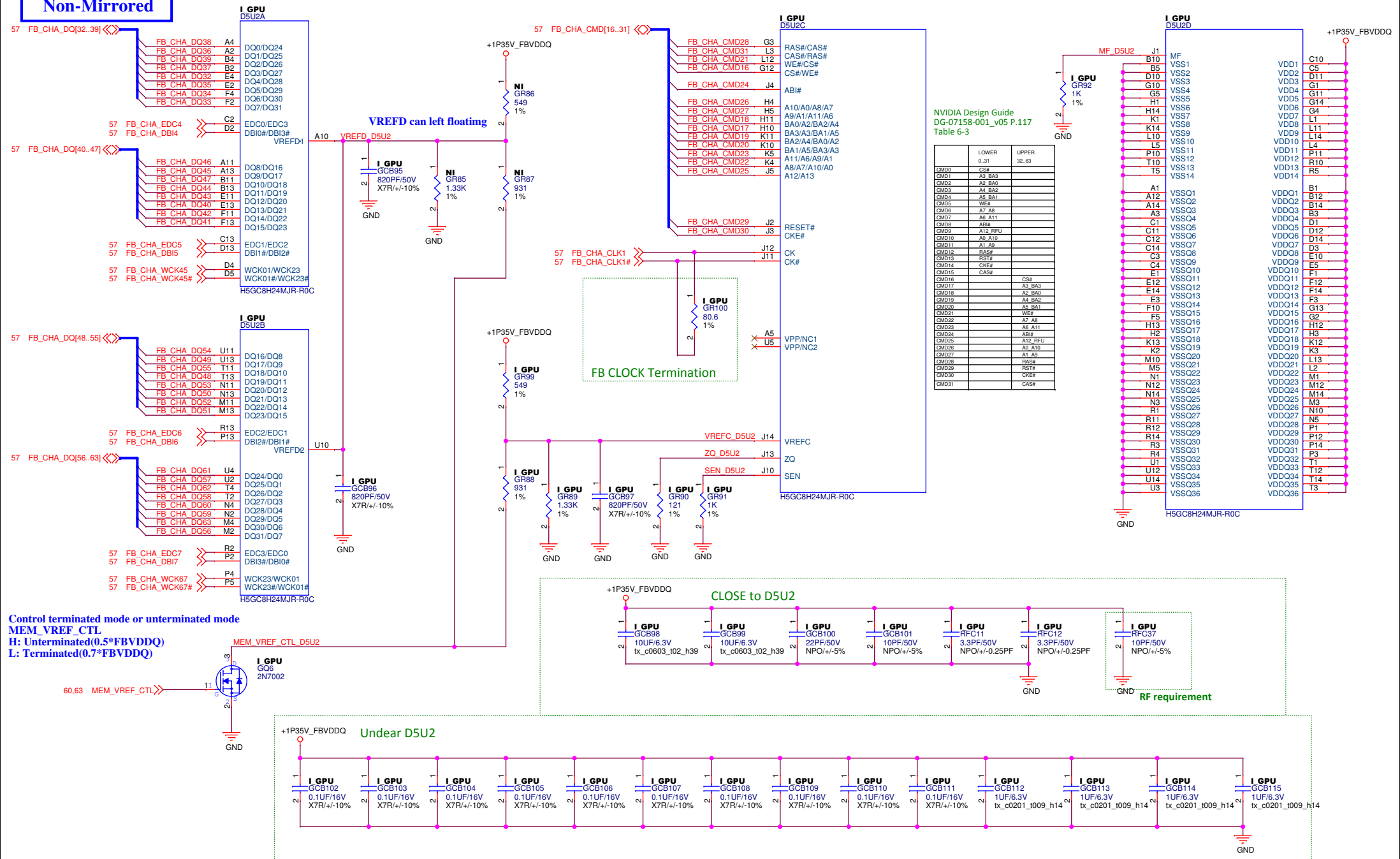
Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111



Non-Mirrored



Non-Mirrored



<Variant Name>

PEGATRON Title : 064 - N16V-GMR1_FB[32..63]

PEGATRON CORPORATION Engineer: *Bacan Hsu*

Size	Project Name	Rev
10	IPV4 CI	...

Date: Thursday, July 25, 2019 Sheet 64 of 97

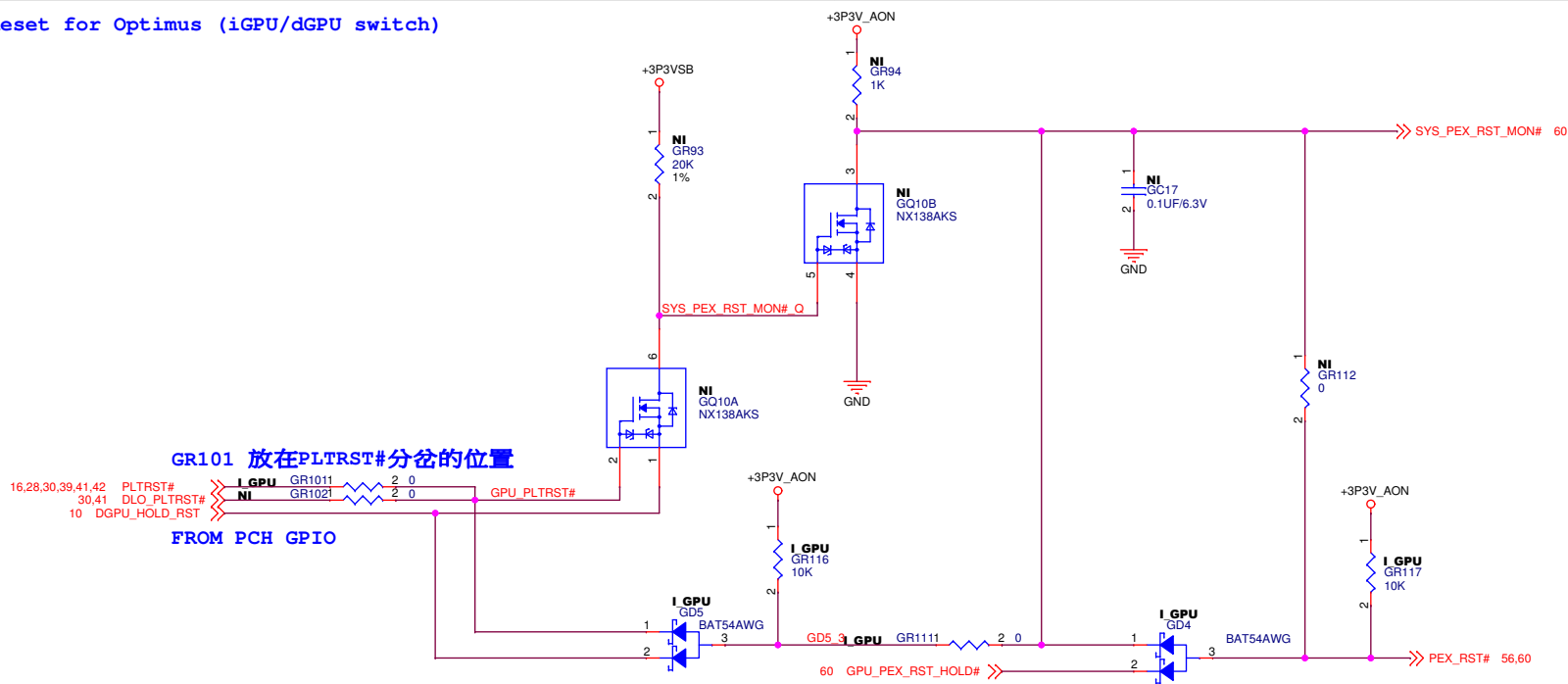
+FBVDDQ decoupling cap for D5U2

0.1uF 0402 X7R 10 Under VRAM

1uF 0603 X7R 4 Under VRAM

10uF 0805 X5R 2 Close to VRAM

Reset for Optimus (iGPU/dGPU switch)



Cold boot:

```
+3P3V_AON --> +3P3V_MAIN --> +NVVDD --> +1P05V_GPU --> +1P35V_FBVDDQ
```

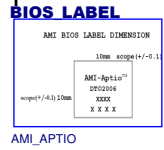
GC6 2.0 Exit:

+3P3V_MAIN --> +NVVDD --> +1P05V_GPU

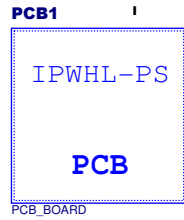
GC6 2.0 Exit:

There is no specific power down sequence

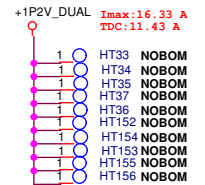
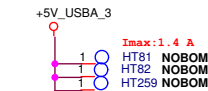
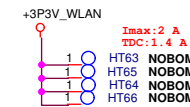
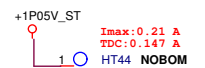
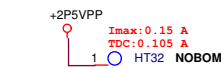
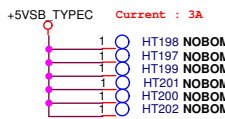
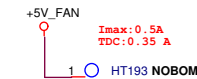
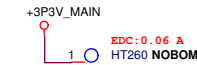
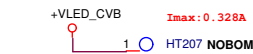
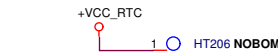
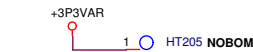
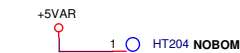
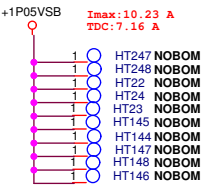
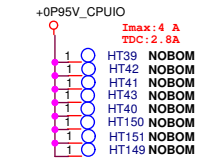
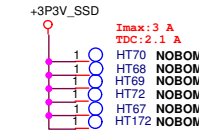
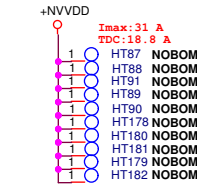
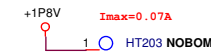
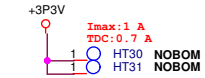
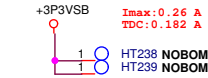
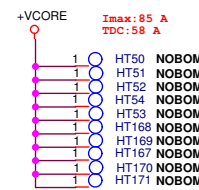
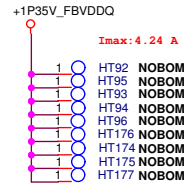
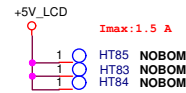
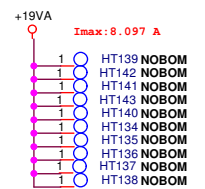
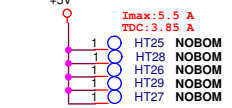
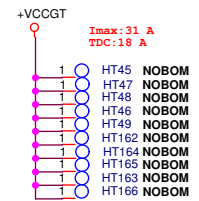
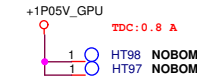
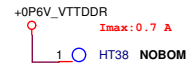
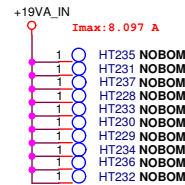
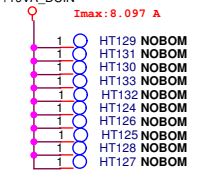
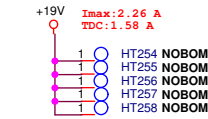
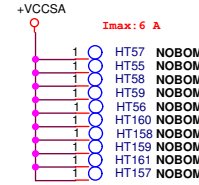
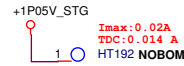
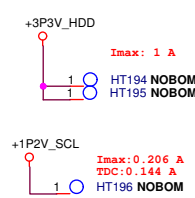
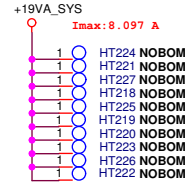
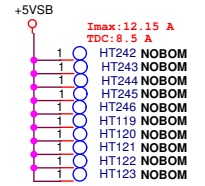
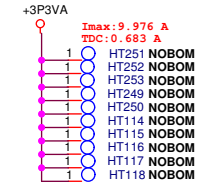
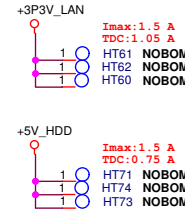
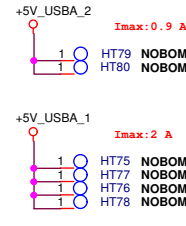
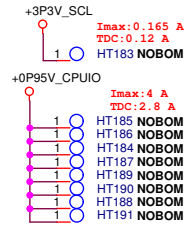
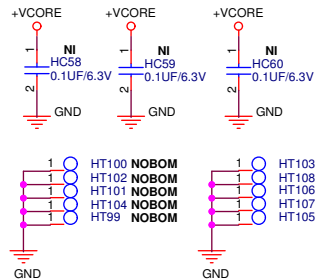
BIOS LABEL

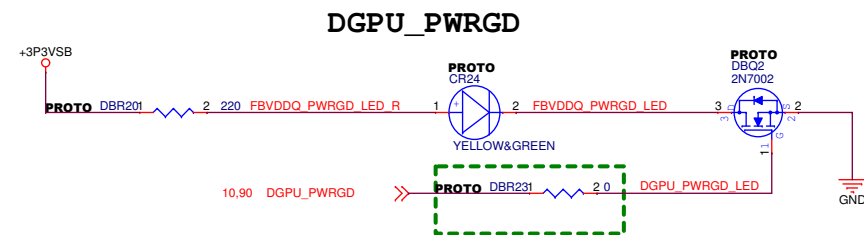
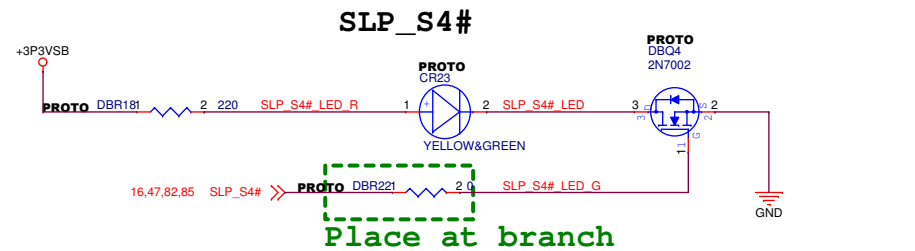
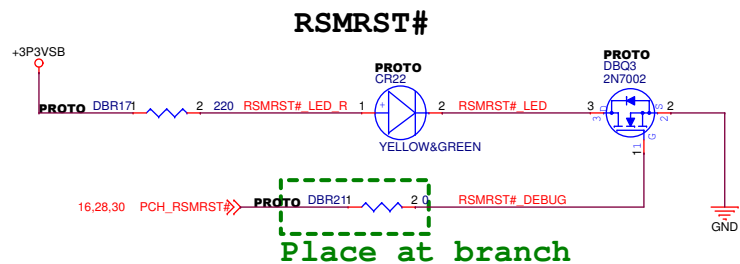
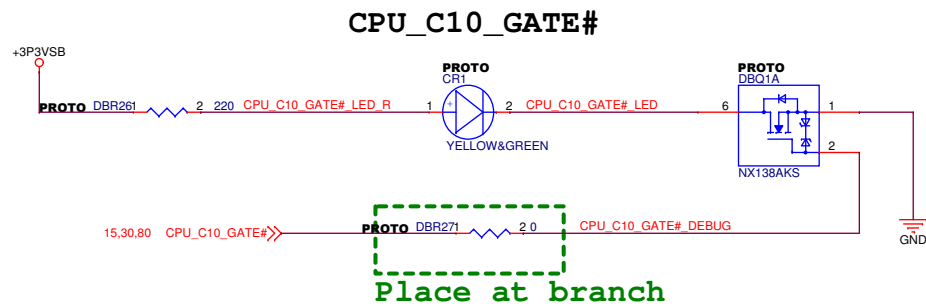
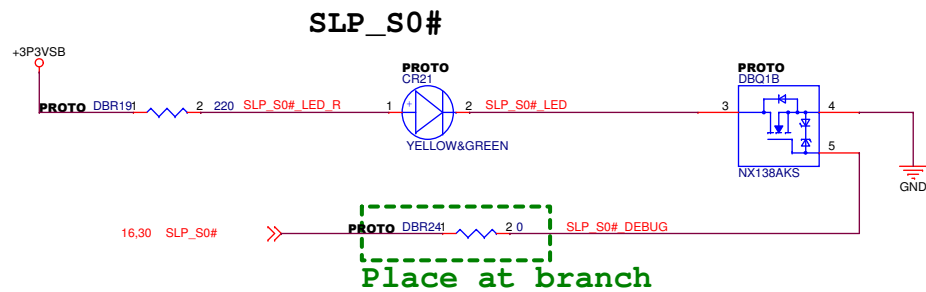


PPID LABEL



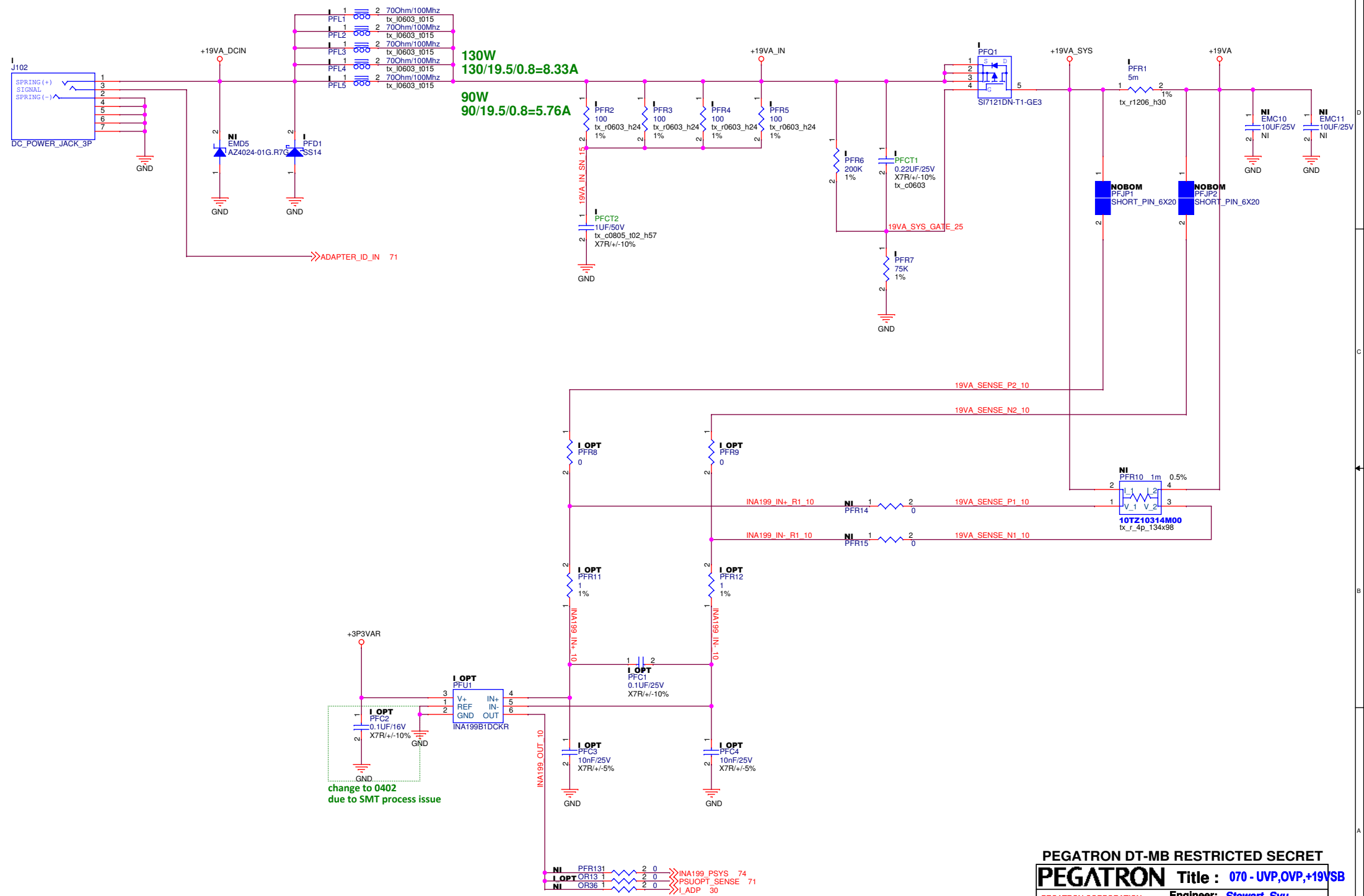
Stitching Caps

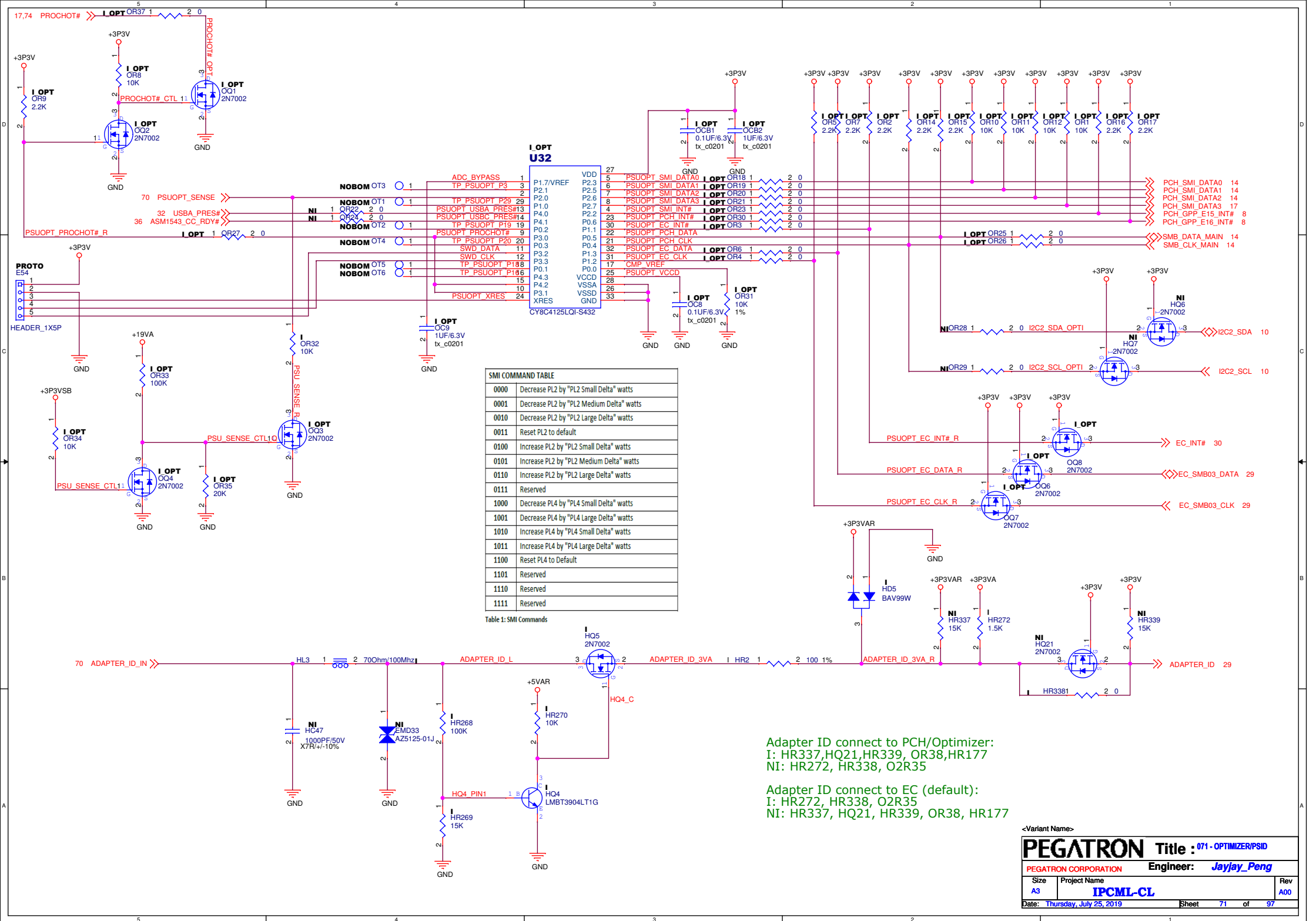


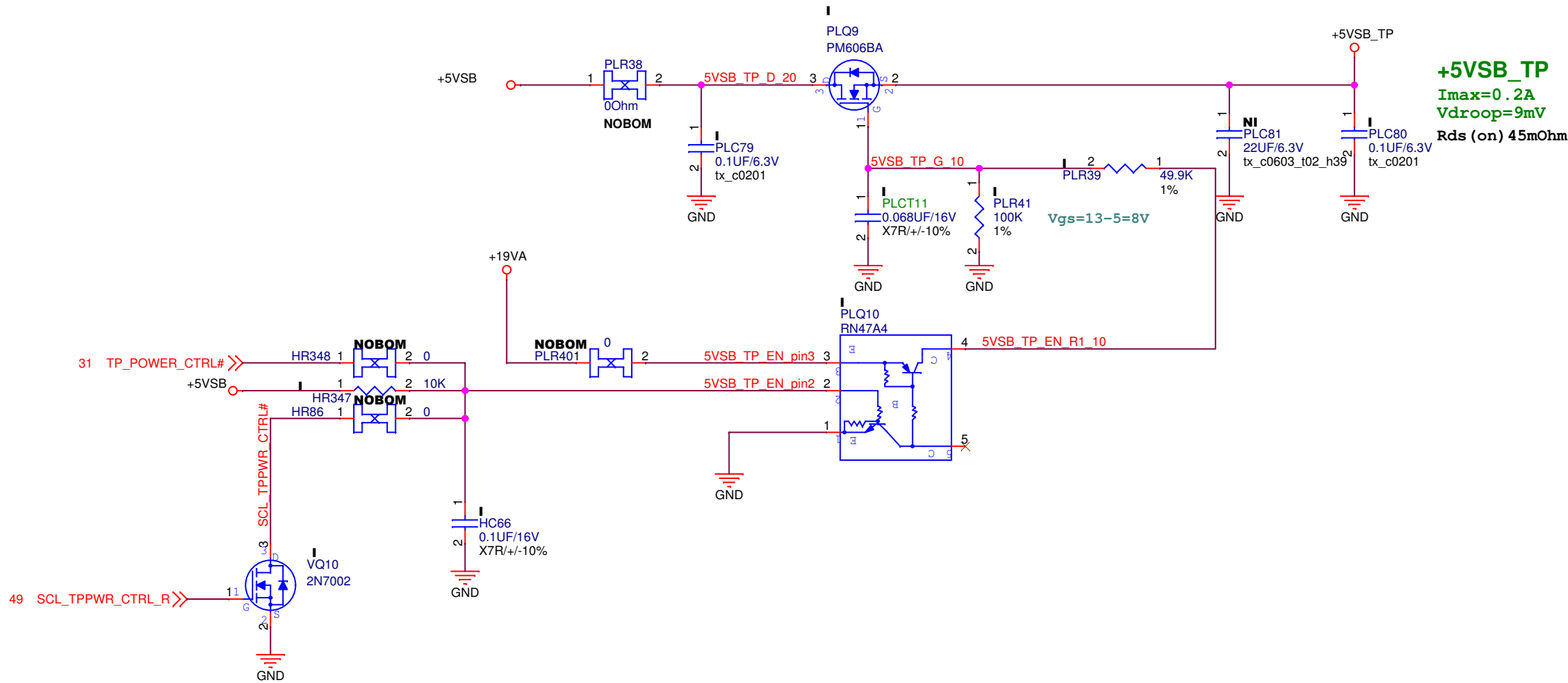


<Variant Name>

PEGATRON		Title : 069 - DEBUG LED	
PEGATRON CORPORATION		Engineer: Jayjay_Peng	
Size A3	Project Name IPCML-CL	Date: Thursday, July 25, 2019	Rev A00
Sheet 69 of 97			

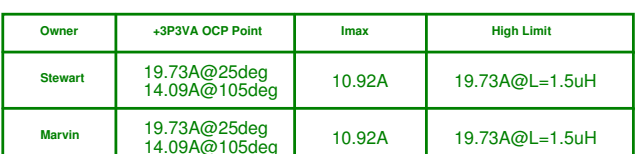






[illegible]

Owner	+3P3VA OCP Point	I _{max}	High Limit
Stewart	19.73A@25deg 14.09A@105deg	10.92A	19.73A@L=1.5uH
Marvin	19.73A@25deg 14.09A@105deg	10.92A	19.73A@L=1.5uH

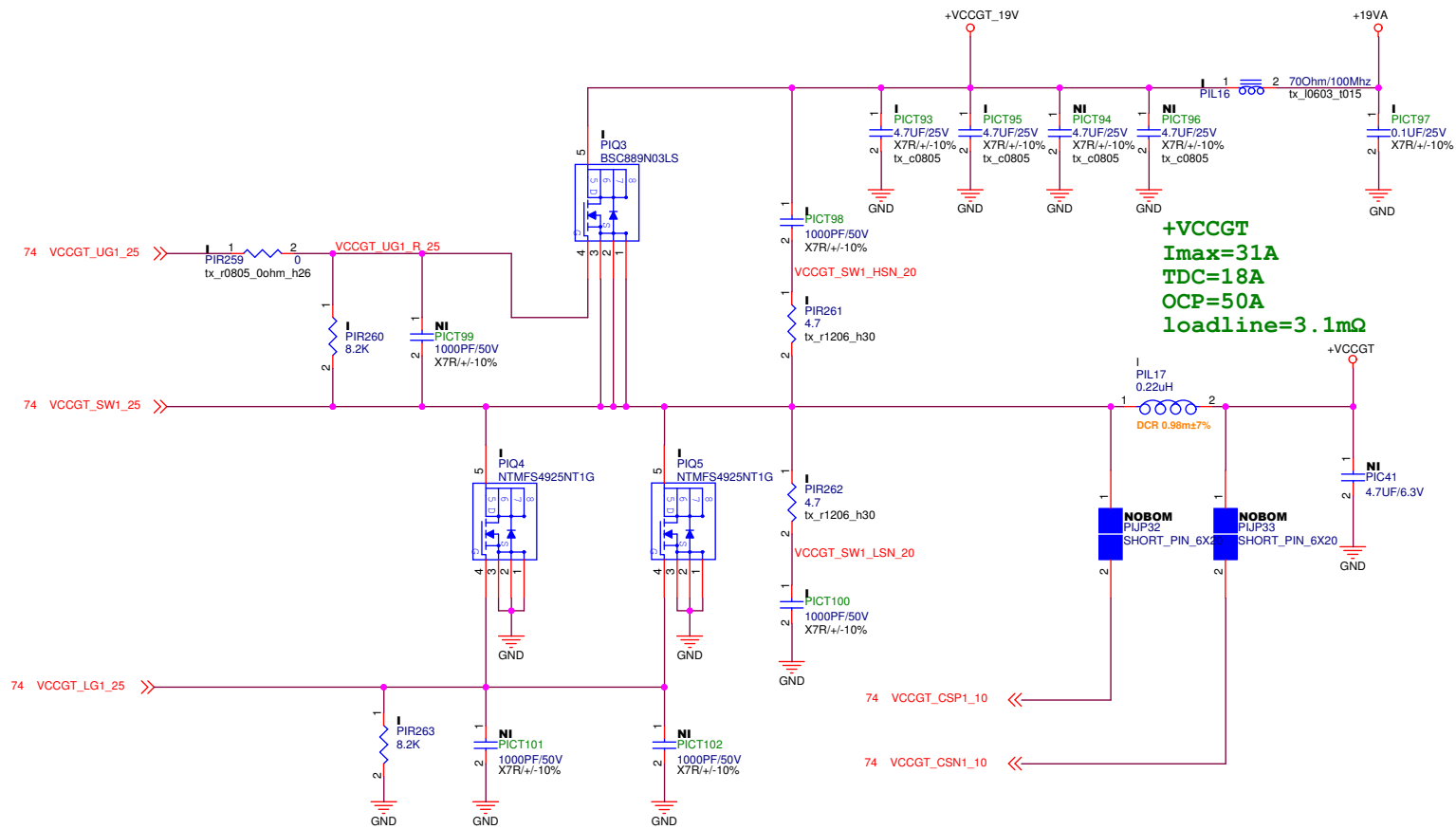




```
+VCORE
Imax=70A
TDC=48A
OCP=105A
loadline=1.8mΩ
```

```
+VCCGT
Imax=31A
TDC=18A
OCP=50A
loadline=3.1mΩ
```

```
+VCCSA
Imax=6A
TDC=4A
OCP=12A
loadline=10.3mΩ
```

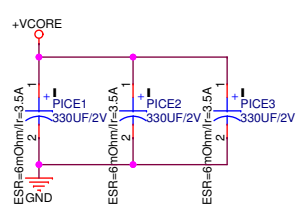



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON Title 076. +VCCGT DRIVER

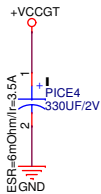
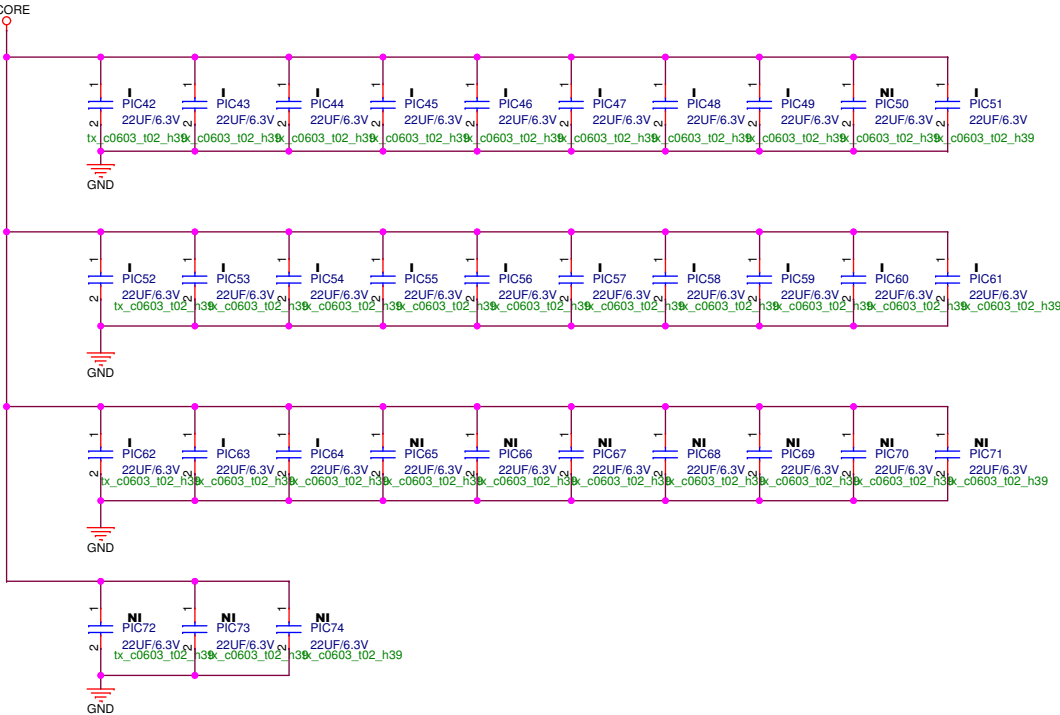
PEGATRON CORPORATION Engineer: Stewart_Syu

Size A3	Project Name IPCML-CL	Rev A00
Date: Thursday, July 25, 2019		Sheet 76 of 97



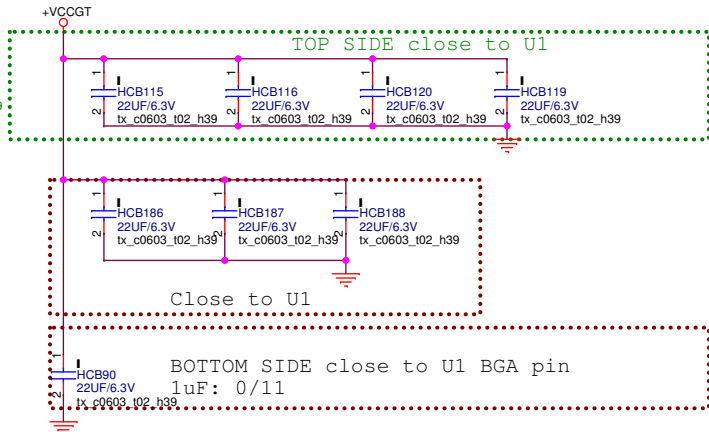
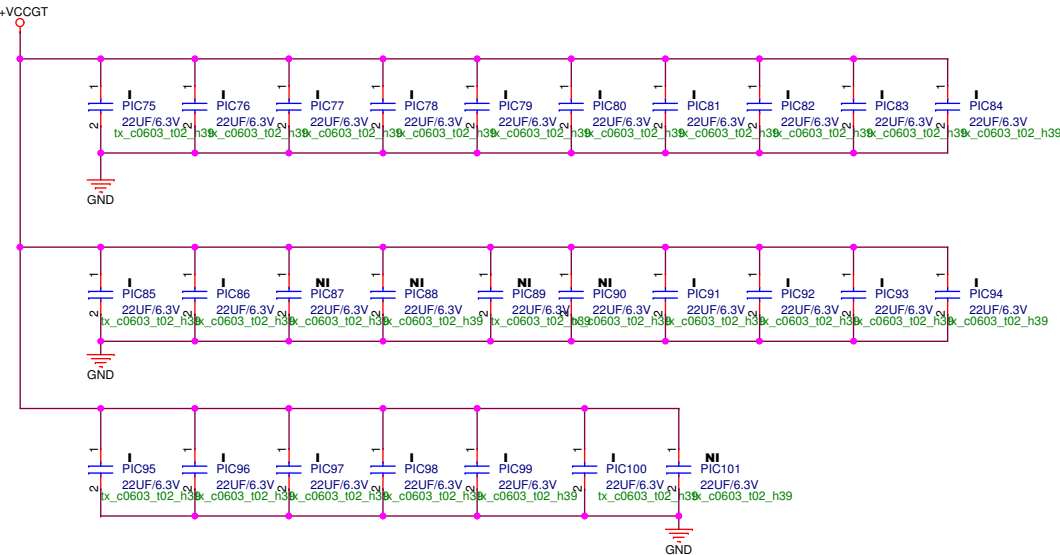
Vcore Output CAP

330uF/2V * 3 pcs
22uF/6.3V * 22pcs



VCCGT Output CAP

330uF/2V * 1 pcs
22uF/6.3V * 30 pcs



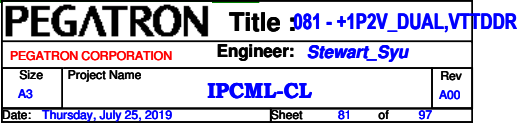
PEGATRON DT-MB RESTRICTED SECRET

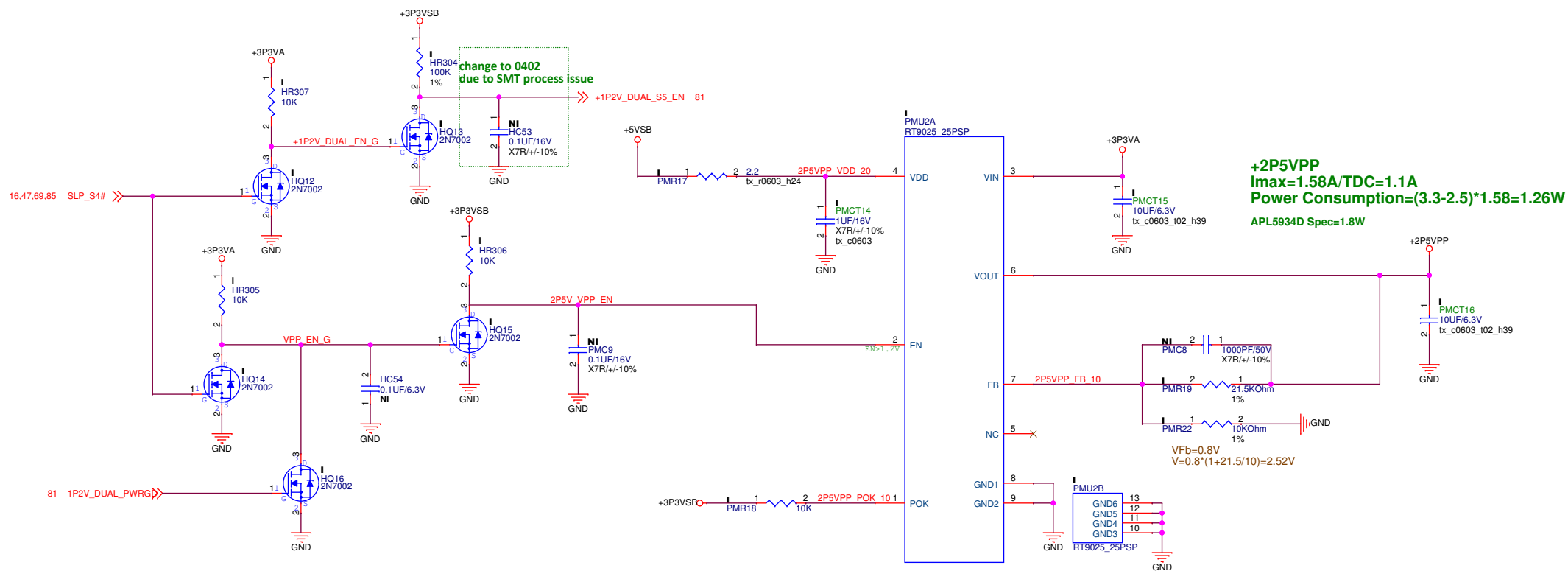
PEGATRON		Title 077. +Vcore & +VCCGT CAP	
PEGATRON CORPORATION		Engineer: Stewart_Syu	
Size	Project Name	Rev	
A3	IPCML-CL	A00	
Date: Thursday, July 25, 2019		Sheet	77 of 97



PEGATRON DT-MB RESTRICTED SECRET

PEGATRON		Title 979. xxx	
PEGATRON CORPORATION		Engineer: Stewart_Syu	
Size A3	Project Name IPCML-CL		Rev A00
Date: Thursday, July 25, 2019		Sheet 79	of 97





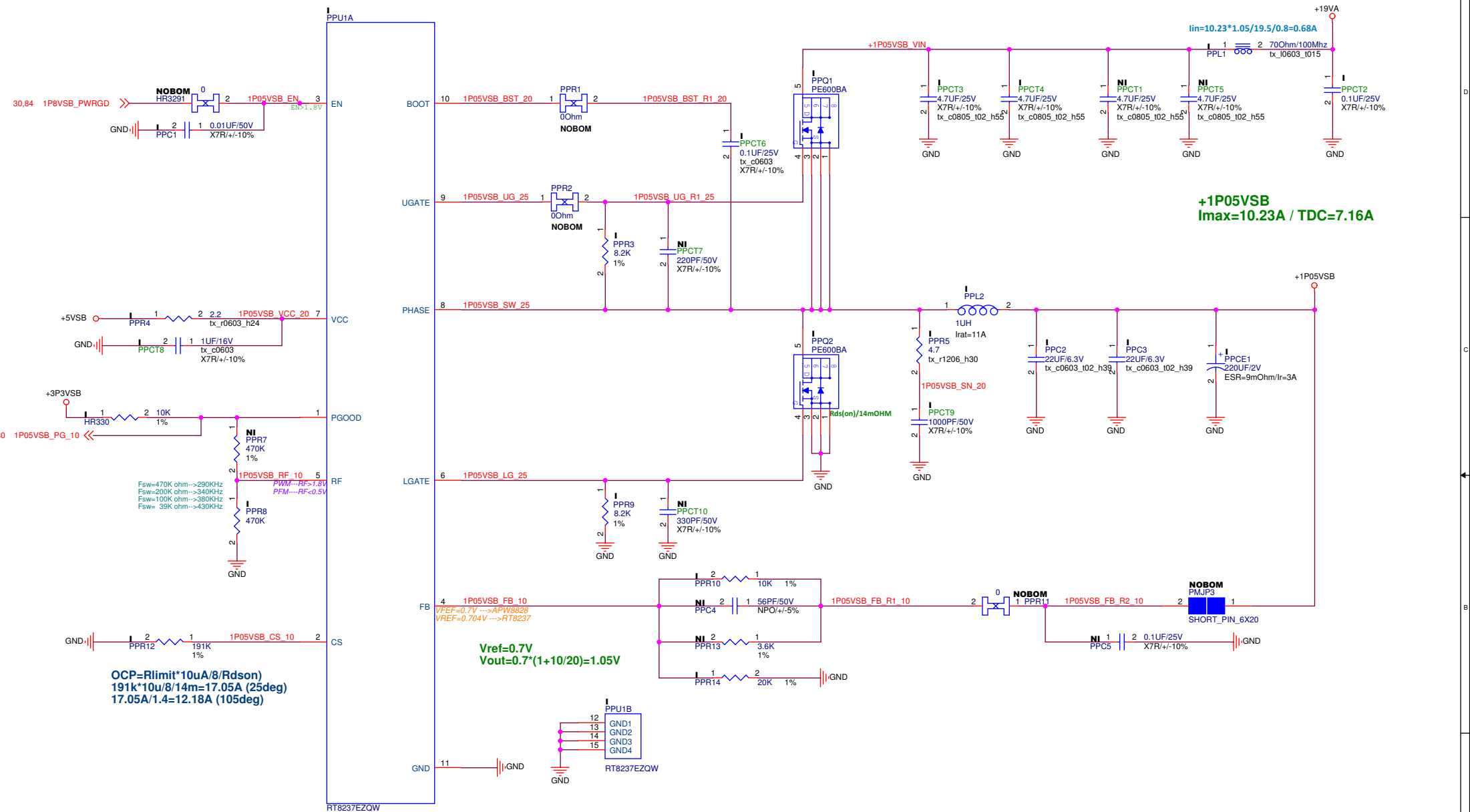
PEGATRON DT-MB RESTRICTED SECRET

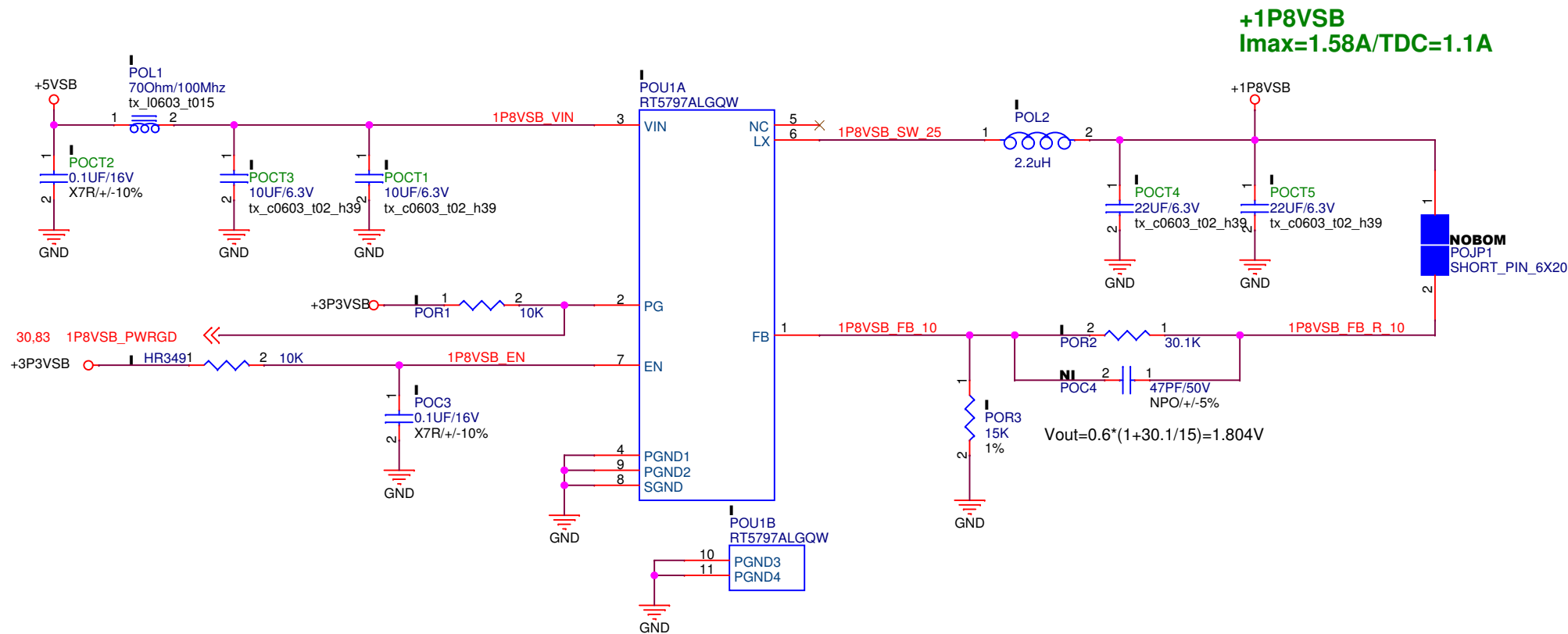
PEGATRON Title :082 - +2P5V_VPP

PEGATRON CORPORATION Engineer: Stewart_Syu

Size A3 Project Name IPCML-CL Rev A00

Date: Thursday, July 25, 2019 Sheet 82 of 97





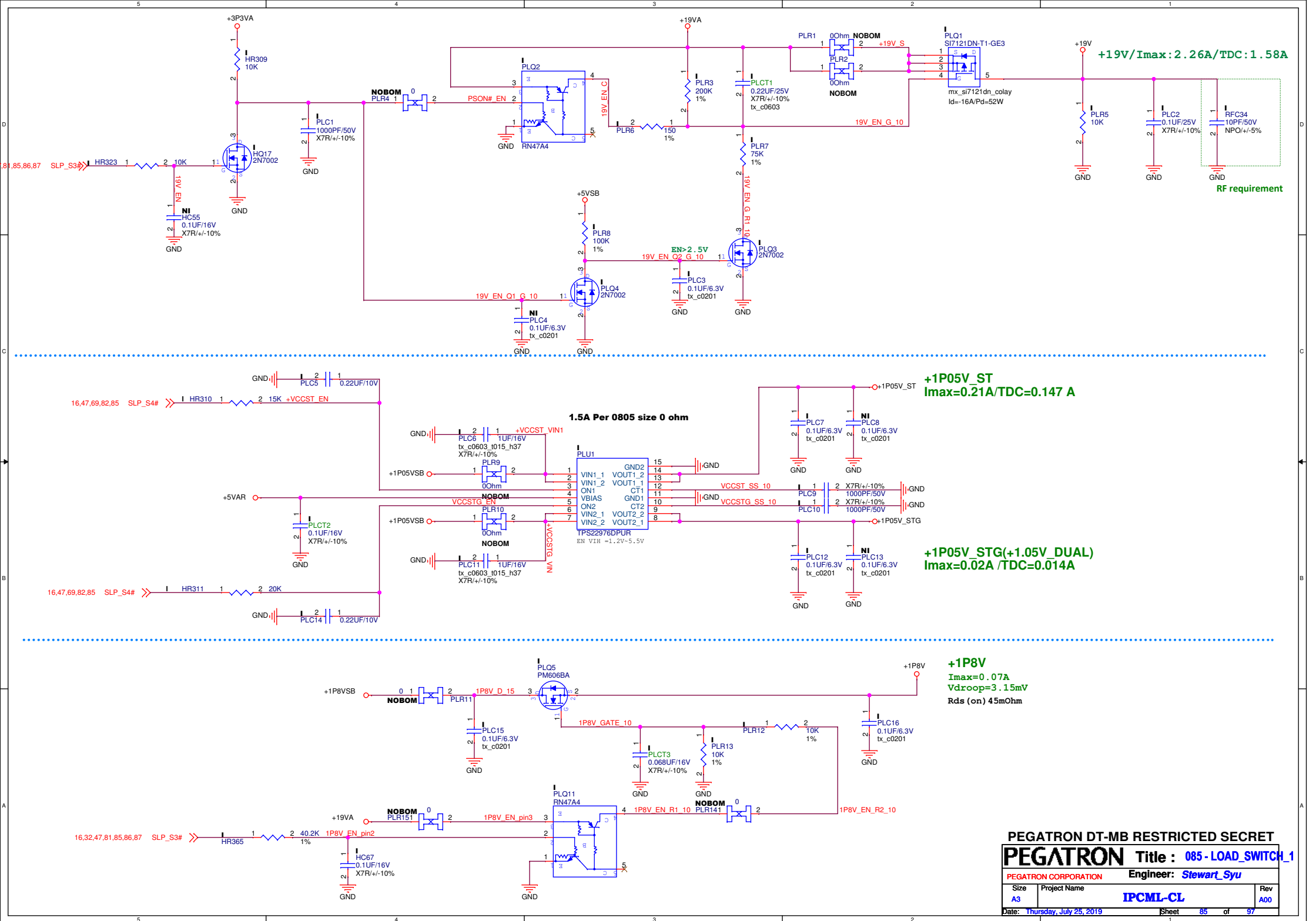
PEGATRON DT-MB RESTRICTED SECRET

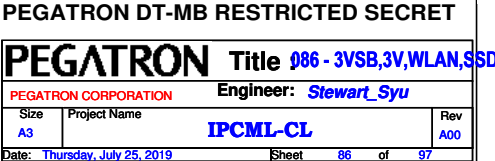
PEGATRON Title : 084 - +1P8VSB

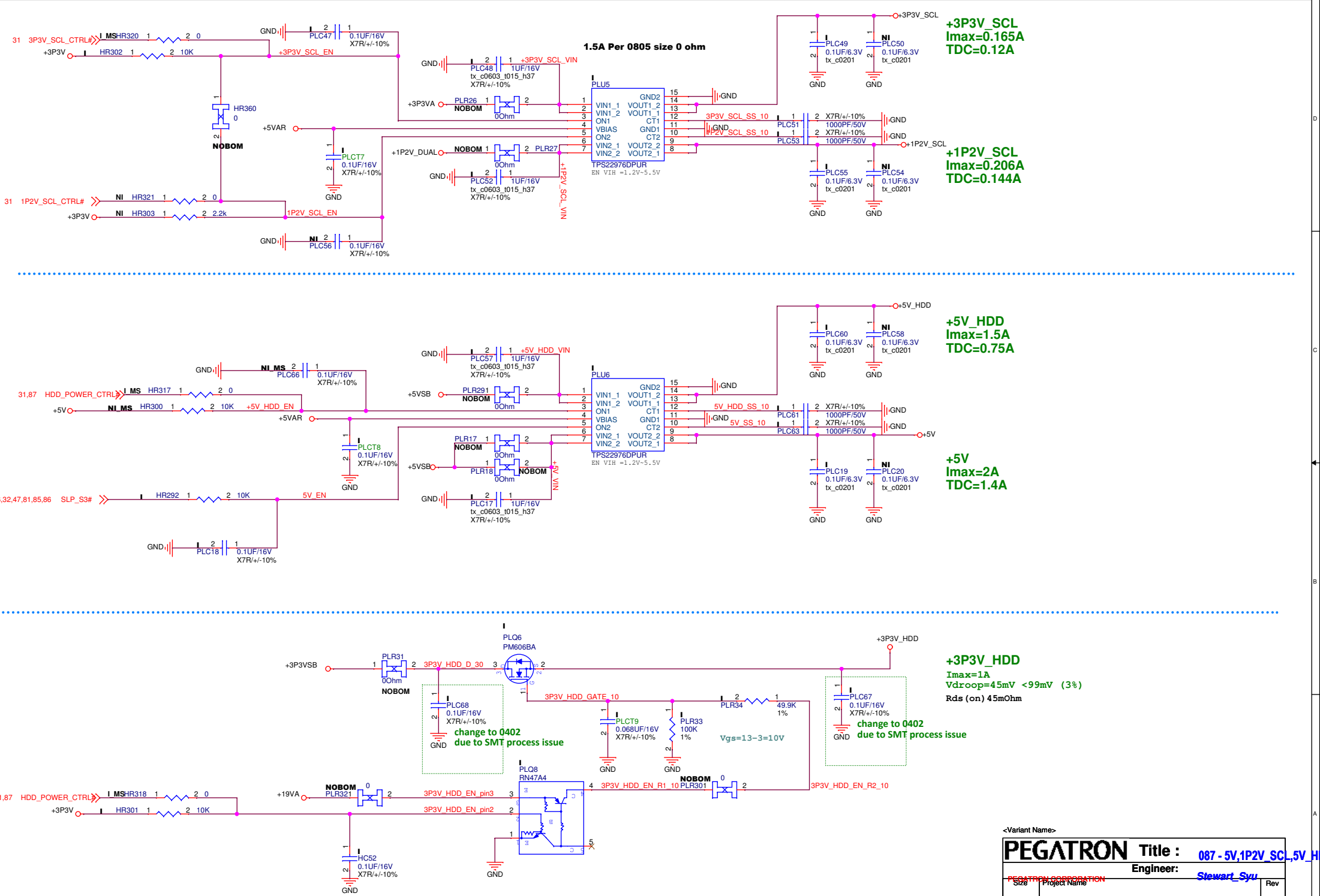
PEGATRON CORPORATION Engineer: Stewart_Syu

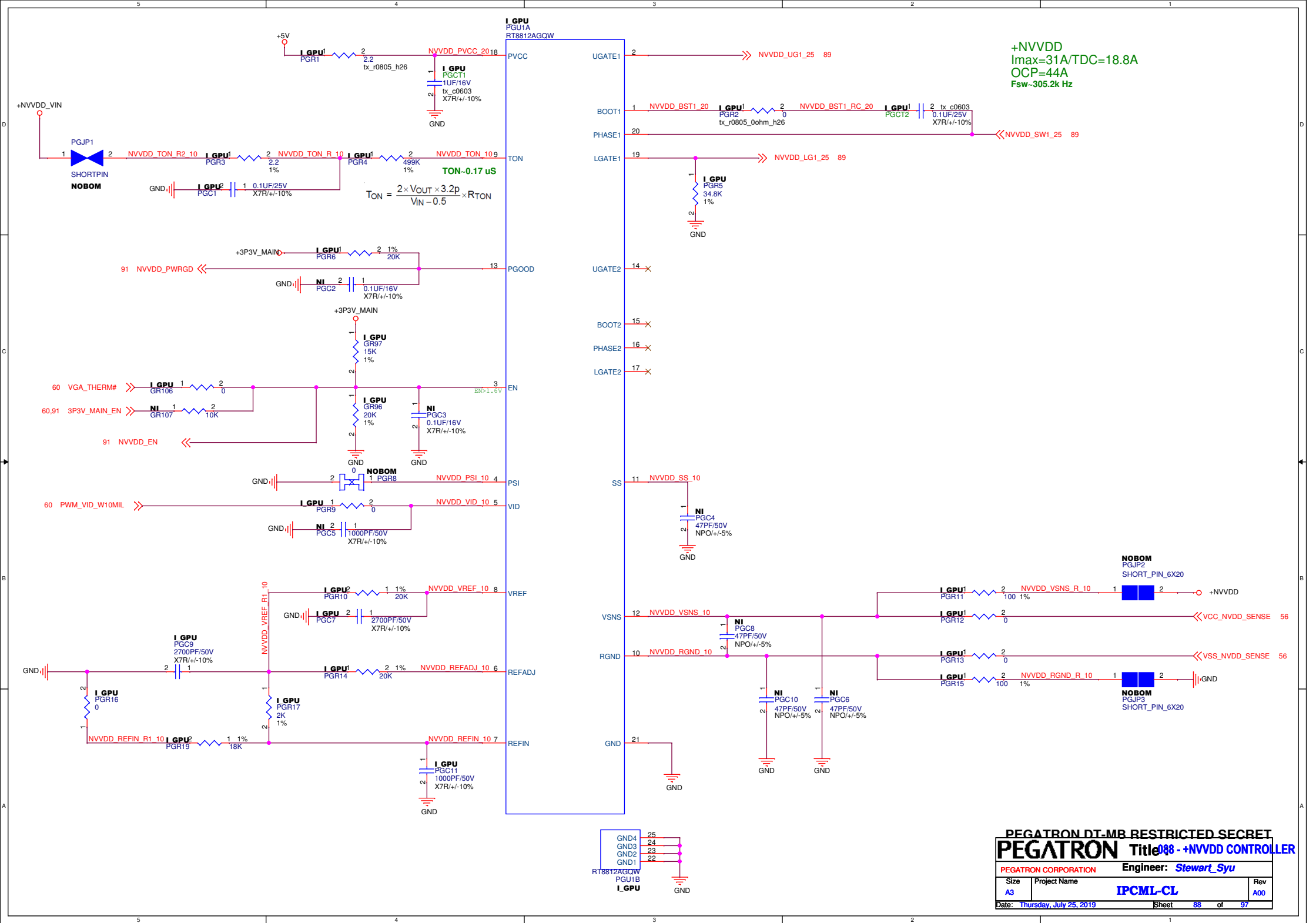
Size A4	Project Name IPCML-CL	Rev A00
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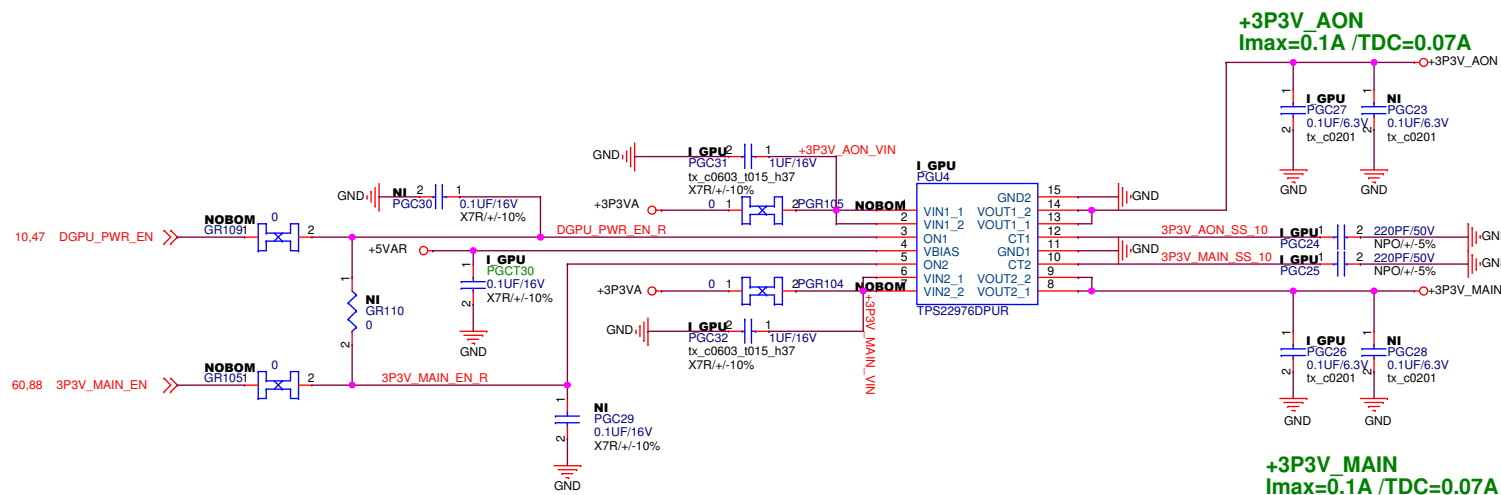
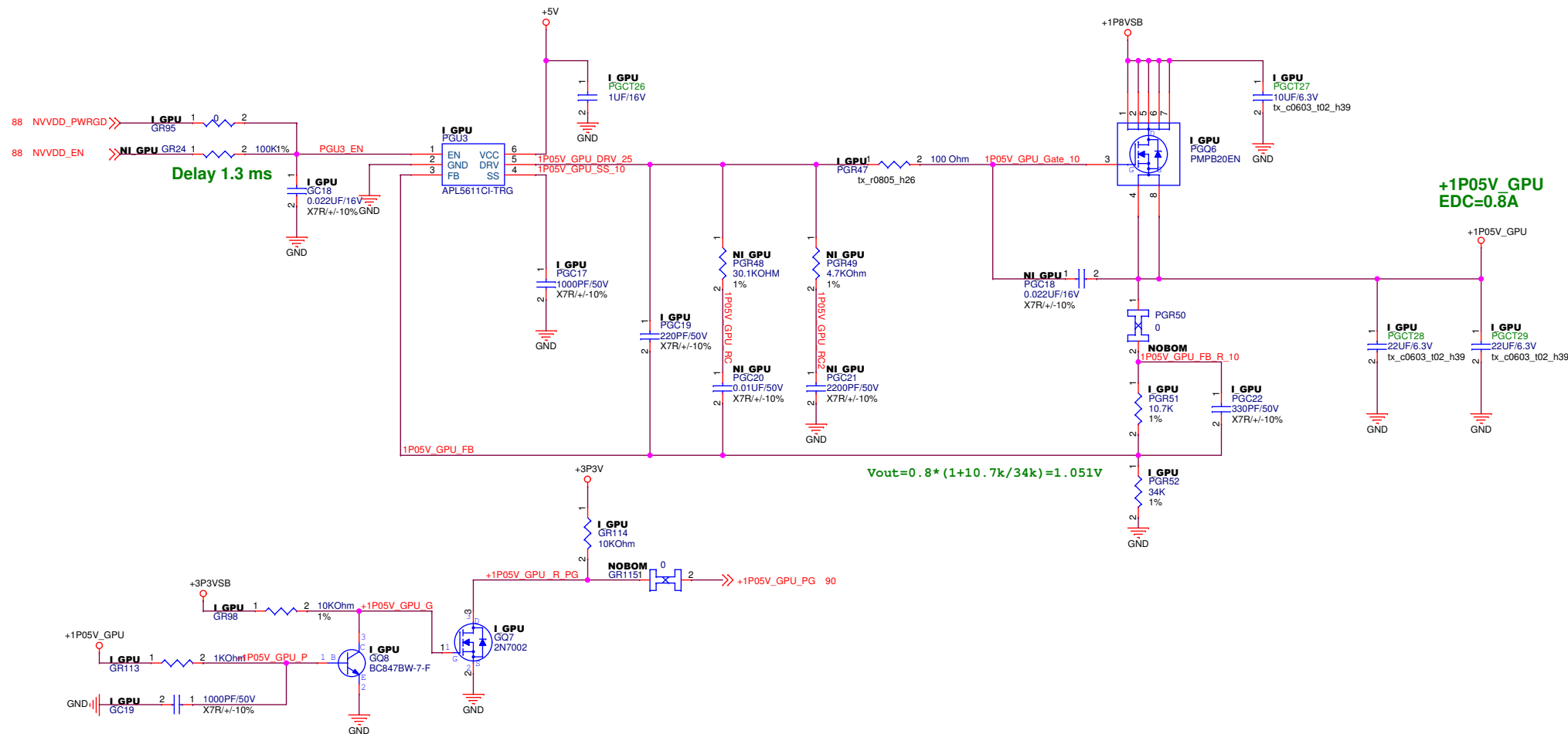
Date: Thursday, July 25, 2019 Sheet 84 of 97

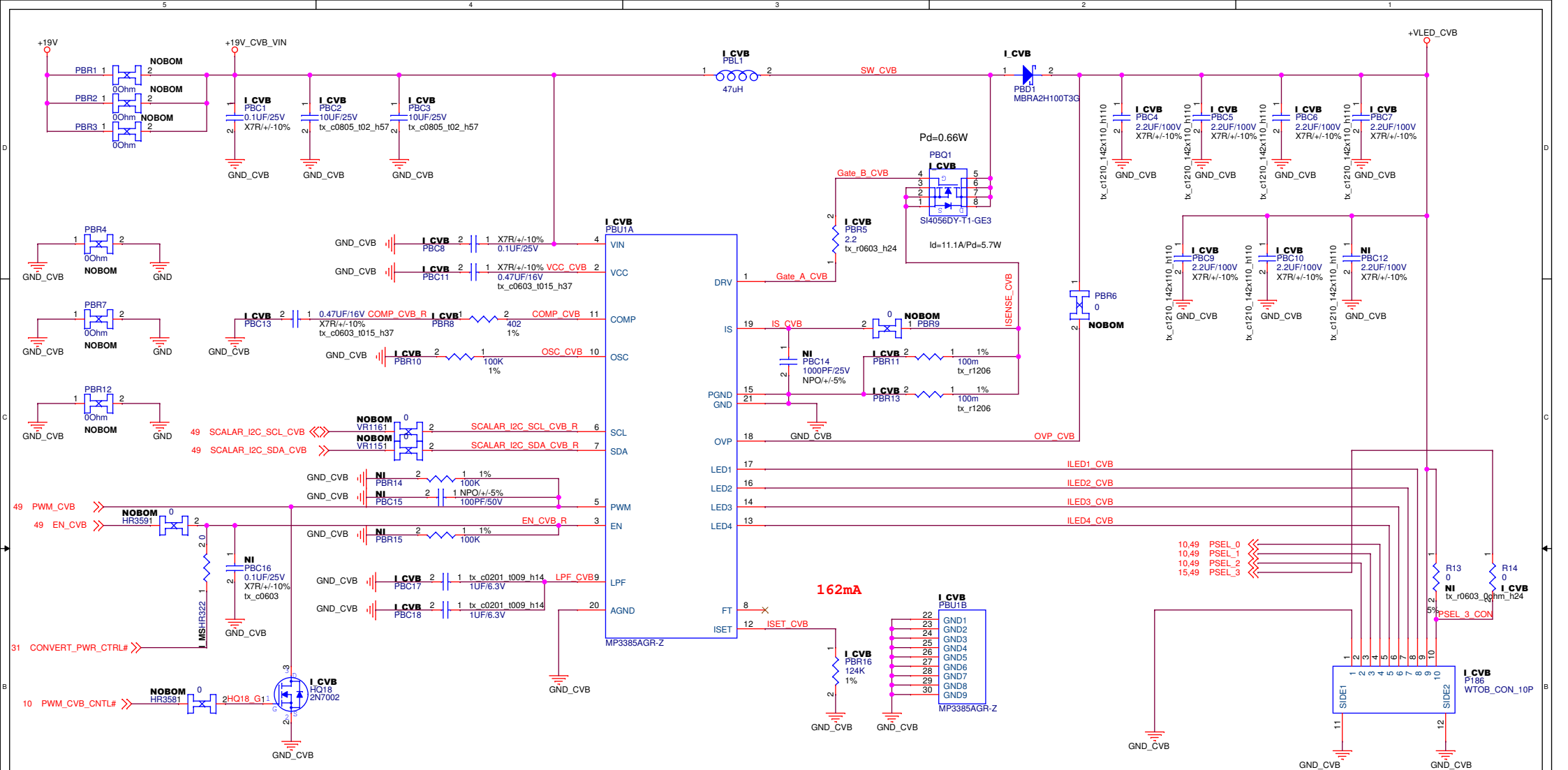












	24'			27'		
Panel	LM238WF2-SSK1	LM238WF5-SSA1	MV238FHM-N20	LM270WF7-SSD1	MV270FHM-N30	
ILED.typ/max	55/60 mA	65/70 mA	53//55 mA	60mA/65mA	57/TBD mA	
VF.typ/max	43.1/46.1V	43.8/46.8V	48.8/51.5V	49.6V/53V	54/57.6V	
OVP.typ	52V	52V	58V	60V	66V	
String	4	4	4	4	4	
ID(0,1,2,3)	0110	0010	1010	1100	TPK OGS 0111	BOE OGS 1001
CABLE	1,4,10(short)	1,3,4,10(short)	1,3,10(short)	1,2,10(short) 1,4(short)	1,2,3(short)	1,2 (short) 1,2,4(short) 1,2,3,10(short)

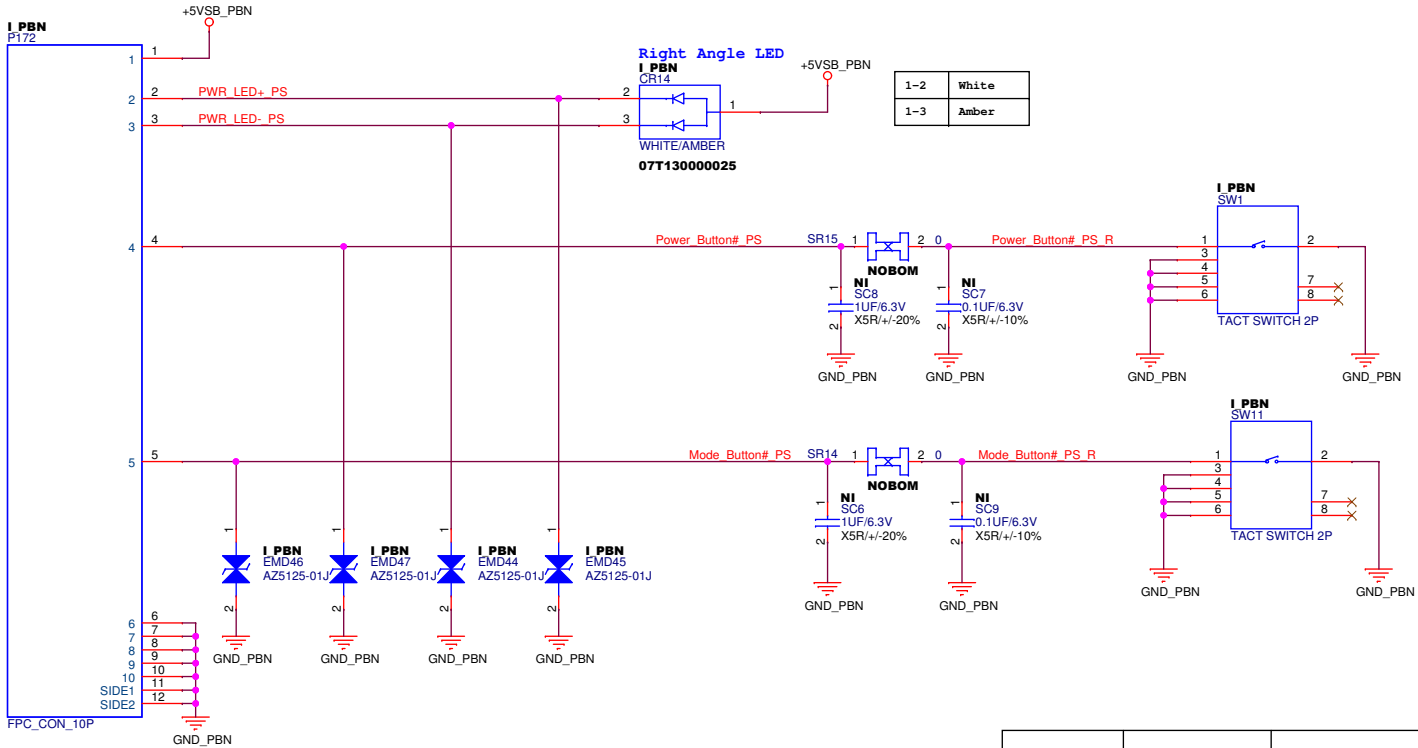
2018-1023 :Update

Breath_LED#	Amber_LED#	WHITE LED	AMBER LED
1	0	ON	OFF
0	1	OFF	ON
0	0	OFF	OFF

10/23 : FPC conn change to white color

PIN2: Breath_LED# 的反向
PIN3: Amber_LED# 的反向

HARVATEK
Amber Vf=1.6V~2.4V
White Vf=2.55V~3.15V



IPWHL-PS
PCB
PCB_BOARD

Schematics Change History

[illegible]